The Jefferson Lab VME-Based High Resolution TDC

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Abstract—**We present the design for a high-resolution time to digital conversion (TDC) module for use in nuclear physics experiments at Jefferson Lab's Continuous Electron Beam Accelerator. Preliminary results on the performance of the prototype and future design goals are discussed.**

I. Introduction

A high resolution TDC module has been designed for use in nuclear physics experiments at Jefferson Lab. The Continuous Electron Beam Accelerator Facility at Jefferson Lab is currently delivering up to 6 GeV electrons to three experimental halls. These experiments currently use FASTBUS based high resolution TDCs that are no longer available commercially. In addition, for many experiments, they become the limiting factor for dead time and event rates primarily because of longer conversion times. New higher rate experiments are also being planned that will place additional demands on data acquisition components. Our TDC design is targeted to meet the requirements of current experiments, as well as address the anticipated needs of future experiments at Jefferson Lab.

A recent trend in large experiments is the design of custom integrated circuits that can perform the desired measurement task. Generally these are low power multi-channel chips allowing them to be mounted directly on or near the detector elements. Many circuits include complex filtering features to suppress data unrelated to the trigger. Some of these integrated circuits have come to be marketed by commercial firms. One such chip is the F1 TDC. This ASIC was originally developed for the Compass collaboration at CERN and is now marketed by acam-messelectronic gmbh [1]. We have designed our TDC module incorporating eight of these integrated circuits.

Our design is implemented as a 6U VME64X slave module. This bus standard was chosen because it is already in use at Jefferson Lab, has good (and evolving) data transfer capabilities, and reasonable channel densities are possible.

II. The TDC Module

A. F1 TDC ASIC

The core of our TDC module is the F1 TDC ASIC. This chip uses purely digital delay techniques to measure time. Each of the pipelined F1 chips provides eight channels at 120 ps LSB or four channels at 60 ps LSB when a reference clock of 40 MHz is used. Internal FIFOs allow for storage of 16 hits per channel in leading and/or trailing edge modes. The following outline pertains to the use of the F1 ASIC in our TDC module.

A key feature of the F1 is a trigger-matching processing unit, which allows for selection of hits within a programmable time window and latency from the occurrence of a valid trigger input. Hits that fall outside of the window and latency settings are suppressed from the output buffer and cleared from the hit FIFO. The trigger-matching feature is used in common start/stop or synchronous measurement modes. In common start/stop mode, a start signal resets the internal measurement counter and a trigger signal sets the measurement window. Hits occurring in time within these two signals will always be accepted by the trigger-matching unit. In synchronous mode, a *Syncres* signal is used to reset the internal measurement counter and thus can synchronize all F1 TDC's being used in an experiment. Internal start signals are automatically generated at a programmable rate. The trigger-matching unit validates hits within the programmed window and latency. Headers and trailers identifying the channel, chip, trigger time and event number can be output to delineate events. The full dynamic range for the F1 is 7.8 μs at 120 ps LSB and 3.9 μs at 60 ps, with a 40 MHz reference clock.

To ensure stability and measurement reliability, each F1 chip is PLL-regulated against temperature drifts and manufacturing tolerances. The feedback loop employs a phase-frequency detector, a loop filter and a voltage regulator, which drives the substrate or core of the F1. In this manner, delays within the internal Delay Locked Loop (DLL) are kept constant which translates into a stable LSB resolution or bin size.

The F1 ASIC is configured via 16 registers that can be accessed through serial interface port. Readout of hit data is via a 24-bit parallel port which is clocked at up to 50 Mhz.

B. Module Architecture

Figure 1 shows a block diagram of the TDC module. The eight F1 TDC ASICs on our module provide 64 channels in normal mode, or 32 channels in high-resolution mode. Front panel input signal levels are differential ECL in order to be compatible with existing systems at Jefferson Lab. Timing control signals are available on the front panel as well as through backplane connections for ease of system integration. A 128K word deep FIFO capable of simultaneous reads and writes is attached to each F1 TDC chip to buffer its output data. The VME interface and all control logic and registers are implemented in a single Field Programmable Gate Array

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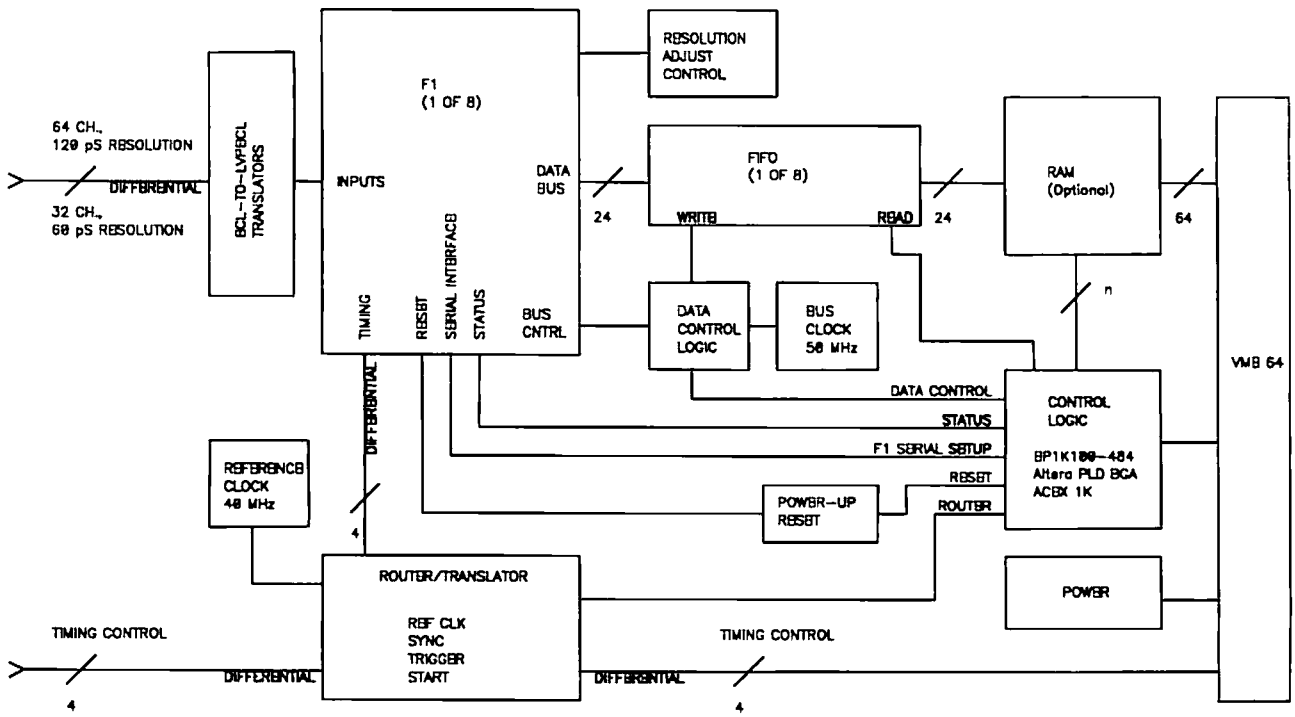

Fig. 1. F1-TDC module schematic

(FPGA). All VME bus transceivers are compatible with the high-speed protocols of the VME64X standard [2]. The RAM shown in Fig. 1 is not present on this prototype. We discuss this option in the section on future plans. In its place a small staging buffer within the FPGA was created to facilitate faster transfers over the VMEBus.

Output data from each F1 TDC is ordered according to channel number (channel 0 first, channel 7 last). Within each channel, hit data is ordered from earliest to latest. We configure each F1 TDC chip to supply a header word for channel 0 and a trailer word for channel 7 in its output data stream whenever a trigger occurs. This takes place even if there is no valid hit data for the trigger. During readout, control logic uses these markers to switch between the FIFOs for each chip. In this way, data from multiple chips that are associated with the same trigger may be assembled into an event fragment for the module. Individual channels may be disabled during configuration of the F1 TDC. The FIFO for an individual F1 TDC may also be bypassed from the readout sequence.

The VME module can be configured to set a flag in a register when the data from a programmed number of triggers is available in its buffers. This flag may be optionally used to interrupt the crate controller. Readout is accomplished most efficiently using a block transfer protocol. Because the number of data words currently stored in the module is not available to the crate controller, a slave terminated block transfer is used. The crate controller is programmed to read out, via block mode, a number of words that is beyond the storage capacity of the module. During readout the module will provide the block of data associated with the programmed number of triggers. When this data is depleted the module terminates the block transfer by issuing a bus error (BERR). A register bit in the module is set when this occurs. The crate controller can query this bit to verify that the bus error was generated deliberately by the module and does not signify a system failure.

To enhance system performance a set of TDC modules may be read out as a single logical read using a chained-block protocol. This involves passing a token between modules along a VME bus daisy-chain line (*e.g.* BG*n* or IACKIN/IACKOUT). All TDC modules in the set are programmed to respond to a common address range used exclusively for chain-block transfers. Only the TDC having the token will actually respond to such an address cycle. The TDC module of the set that is furthest left in the crate is configured to be the first module and initially claims the token. The module furthest to the right is set as the last module. All modules except the last one are configured to pass the token when they have transferred the programmed number of events. The last module is configured to respond with BERR. (Caveat: Recent manufacturing changes in some VME64X backplanes now include active logic requiring participation of the bus arbiter or daisy-chain controller. Older backplanes relied on mechanical jumpering or auto-jumpering connectors. The active backplane effectively defeats the above technique for multi-cast and chained-block transfer in these crates. The authors are currently investigating workarounds and alternatives.)

C. Configuring the F1 TDC ASICs

The TDC board contains eight F1 devices that must be configured prior to operation. Each device contains sixteen 16-bit write-only configuration registers accessible through a synchronous serial bus. During normal operation these registers, once programmed would not be changed. However, the user may need random access both for status and modification. To facilitate this the TDC configuration control logic is implemented in the FPGA. It contains a serializer for the F1, a register file RAM, a configuration sequence RAM, an EEPROM controller, and host interface logic. Read-back is accomplished using a local copy of the registers stored in FPGA RAM. A 128x16 register file RAM stores all 16 registers from each of 8 F1 TDCs. Any write to the register file will store the data in RAM and serialize the data to the F1 ASICs. The serializer will construct the F1 data frame based on the register file address and write data.

A 512x8 serial EEPROM stores the sequence RAM and other user data even when the module is not powered. The EEPROM is accessed through an EEPROM controller and an SPI compatible interface. The controller provides a random access read/write interface to the EEPROM. It manages device opcodes, status, and data. The SPI interface contains a clock manager and a serializer/deserializer. Since the Sequence RAM and end address occupy only 385 bytes of the 512-byte EEPROM, the remaining space is available for user data.

The Master Controller module provides a host interface to the control logic and interconnects the register file, sequencer, and EEPROM modules. It permits read and write access to the Register File RAM, Sequence RAM, and EEPROM. The host can trigger TDC configuration from Sequence RAM and transfer of Sequence RAM to or from the EEPROM. At power-up, the Sequence RAM and end address are automatically loaded from EEPROM then passed to the register file and serializer to configure the F1s. This automatic power-up configuration will remove considerable software overhead for a large number of TDC boards.

D. Implementation

The TDC module is fabricated as a single 12-layer printed circuit board. Signal characteristics are preserved throughout the front end of the circuit board by extensive use of differential PECL strip lines. The strip lines are properly sized for 50 Ohm termination and to provide proper signal deskewing. Except for connectors, components are surface mounted using both sides of the board. The module uses +3.3V and thus requires a VME64X backplane. Total power dissipation is 38 W.

With the high power dissipation of the VME module there is concern for heat related issues. The F1 ASIC, when overheated, can lose the PLL lock and become disabled. The close proximity of eight F1 ASICS all active on a single board requires substantial fan cooling. We are also investigating the use of heat sinks in order for all F1s to operate at their highest adjustable resolution.

III. Measurements

A. Test Setups

For a majority of the tests (calibration, resolution, crosstalk) we used a Highland V851 Digital Delay Generator [3] as our signal source. This VME module drives up to six outputs with programmable delays relative to a reference output T0. All outputs are NIM levels. Four of these outputs are fanned out 8 ways to create 32 timing signals. These are converted to ECL levels and serve as inputs to 32 of the TDC module channels. The T0 output is converted to ECL and is used as the *Start* input to the TDC. Another output is converted and is used as the *Trigger* input to the TDC. This setup allows us to study up to half of the TDC module channels simultaneously.

The delay of *Trigger* relative to *Start* is fixed to be slightly less than the full dynamic range of the F1 (3.9 μs or 7.8 μs). delays of the four source signals (from which the 32 input timing signals are derived) are adjusted to study the TDC response. Trigger matching mode is enabled for the F1 ASICs, with latency and window parameters programmed to be slightly less than the *Trigger* delay.

With this setup the module functions as a multi-hit common start TDC. All hits on an input channel that occur between the *Start* and the *Trigger* times will be measured.

The quality of the TDC test signals was checked with the Stanford Research System SR620 Time Interval Counter [4]. The SR620 has a resolution of 25 ps. The jitter of the TDC test signals relative to *Start* was measured to be 33 ps (RMS). The SR620 also confirmed the linearity of the V851 over the range in which it was used.

Additional tests were performed using an NIM module from Berkley Nucleonics Corporation. The DB-2 Random Pulse generator [5] provided up to 1 MHz input rate for multi-hit and differential linearity measurements over the F1 full dynamic range.

B. Results

Fig. 2 shows a typical timing distribution for an input signal with a fixed (delayed) relationship with the *Start* signal. Both normal and high-resolution modes are shown. The quoted RMS values for both modes include systematic uncertainties from the test equipment (*i.e.* digital delay, NIM-ECL translators). They were consistent within uncertainties over the full range of the F1 in both modes. Linearity of the F1 resolution over the whole dynamic range for a single input is shown in Fig. 3.

Histograms displaying differential linearity are shown in Figs. 4 and 5 for both normal and high-resolution modes. Both indicate a flat response overall. However, in high-resolution mode there is a substantial non-linearity for the LSB. This behavior in the F1 was previously noted by Acam and is within chip specifications. So it seems not to be a board design issue.

Preliminary tests on the prototype indicate a general pattern of crosstalk that is consistent with shifts occurring within a single F1 chip. No significant crosstalk effects were seen on inputs that did not share a common F1. Table 1 shows the relationships of four inputs into a single F1. The chip is operating in high-resolution mode. Both the maximum magnitude of the shift as well as the relative delay window for the shift is indicated. Similar results were seen for all other chips tested.

While the inter-channel influence is not negligible, it is small, and the window of effect is narrow with respect to the full dynamic range of the F1. A well understood pattern for the influence could also be used to design a detector interface accordingly.

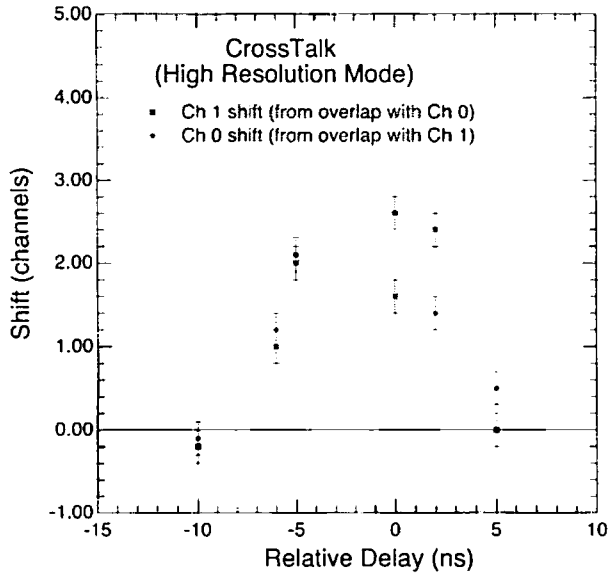

Fig. 6 Crosstalk effects for two adjacent inputs on a single F1 chip. A one channel shift represents 60 ps.

TABLE 1
CROSSTALK EFFECTS (MAGNITUDE AND WINDOW)

Inputs	0	1	2	3
0		+2.4 Ch -10ns - +5ns		
1	+2.6 Ch -10ns - +5ns		-1.5 Ch -5ns - +5ns	
2				+4.0 Ch -10ns - +5ns
3			+3.6 Ch -10ns - +5ns	

IV. FUTURE PLANS

Testing the performance of the F1 TDC chip in this environment will continue. Two additional prototype boards have been built. Tests with multiple board systems including chained-block transfers, crate heat loading, and fan cooling are underway.

The ability to transfer data quickly from the VME module to a CPU for processing is critical, particularly for future experiments. The VME interface of the prototype will be upgraded (by firmware) to include the 64-bit (80MB/s) and dual-edge (2eVME 160MB/s) data transfer protocols. The next version of the F1 TDC module will include a large RAM buffer shown in Fig. 1. It will be organized as 1M x 64 bits to take advantage of the 64-bit data transfer modes of VME. Until then resources on the Altera FPGA allow for a small VME staging buffer (4KB) to be created. This speeds up all block transfer modes by decoupling VME readout from the eight event FIFOs. With the progressing commercial support of existing VME standards (through vendors such as Motorola [6]), we ultimately plan to move to dual edge source synchronous transfers (2eSST 320 MB/s).

We anticipate the VME form factor to be viable for nuclear physics experiments for a long time to come. Future experiments at Jefferson Lab are expected to place much more demand on data acquisition performance. Our plan is to move towards a "dead-timeless" fully pipelined front-end. The F1 TDC represents one step in that direction.

V. ACKNOWLEDGMENT

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VI. REFERENCES

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[7] GlueX Collaboration, http://www.gluex.org.