F1 TDC test (1)

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T. Miyoshi

1 Purposes

Purposes:

1 : time gate width check

2 : long term stability (time resolution)

3 : trigger rate stability (time resolution)

4 : cross talk check

L1 output from trigger module (TIR) is sent to some f1 tdc inputs and the trigger input. A signal is put in slot 12 ch 32 as the reference (start) signal. The other signals are sent to the other channels with high resolution mode ($\sim$ 57 ps/ch).

Clock signals are used for the trigger.

All the measured time is trigger time itself at slot 12 - ch 1 to 16, the 5th f1tdc (f1tdc are slot 3,4,5,6 and 12).

See hid = 52 ("ch 257") to 79("ch 288") in HBOOK file.

2 Run summary

3 Time gate width

Run 1733 has about 900 k events. Programmable resolution setting is 113.2 ps/ch. TDC range is from 45 to 64557, so the full width is 64512 (the full range is 7.3 us). This value is used for time correction in analysis. Note that the gate setting to accept signals is 1 us just before a trigger signal.

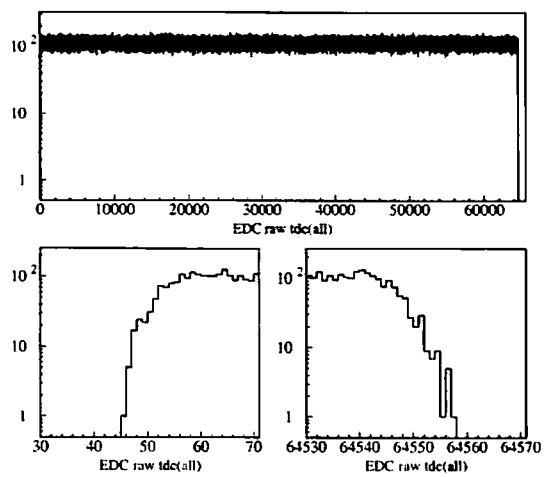

Figure 1: Raw TDC spectrum for signals in f1 chip 1 in tdc range check

Run No.	Fan-in/out output	F1TDC input ch. slot 12	Trig. rate	Resolution	Remarks
1733	1-4	1-4	10^3 Hz	high	900k events (tdc window check)
1736	1	1	10^3 Hz	high	start rate test
1737	1	1	10^4 Hz	high	
1738	1	1	10^2 Hz	high	
1765	1	1	10 Hz	high	
1769	1	1-4 (one by one)	10^3 Hz	high	start crosstalk test
1770	2	1-4 (one by one)	10^3 Hz	high	ch1,2 at the same time
1771	1 to 1ch 2 to 2ch	1,2	10^3 Hz		
1772	1 to 1ch 2 to 3ch	1,2	10^3 Hz		
1773	1 to 1ch 2 to 4ch	1,2	10^3 Hz		
1780	1	1,5(one by one)	10^3 Hz		
1781	2	1,5(one by one)	10^3 Hz		
1784	1 to 1ch 2 to 5ch	1,5	10^3 Hz		
1795	1 to 1 2 to 2	1,2	10^3 Hz	High	ch2 16 ns delay
1794	2	2	10^3 Hz	High	ch2 16 ns delay
1797	2	2	10^3 Hz	High	ch2 32 ns delay
1798	1 to 1 2 to 2	1,2	10^3 Hz	High	ch2 32 ns delay
1799	1 to 1 2 to 2	1,2	10^3 Hz	High	ch2 48 ns delay
1800	2	2	10^3 Hz	High	ch2 48 ns delay

Table 1: Test run summary

4 Long term stability

Run 1765 was took for one night, $\sim$ 18 hours with low-rate (10 Hz). Time resolution is unchanged compared with short-time high-rate (1 kHz) runs.

5 Trigger rate stability

Time resolution is unchanged with trigger rates 10 - 10000 Hz. Check hid=52 at the run 1736 to 1738 HBOOK files for the confirmation.

6 Crosstalk

Crosstalk is not negligible with time measurement using scintillators. Two signals are put into two f1 inputs at the same time (the difference should be less than 500ps). Although channels are shifted, time resolution is not changed. There is no crosstalk between chips. Two Adjacent or both-sides scintillator signals should be put into a channel in one chip and another.

When ch2 is delayed from ch1 by more than 32 ns, channel shift at ch2 become less than 1.

In the normal resolution mode, time is shifted by 1 ch when the same timing signals are put into ch 1 and 2. However, this is negligible for drift chamber measurement compared with drift time width $\sim$ 100 ns.

ch & ch	Shift(ch)	Remarks
1,2	+4,+3	chip 1
1,3	+1,-2	chip 1
1,4	+1,-1	chip 1

Table 2: Crosstalk

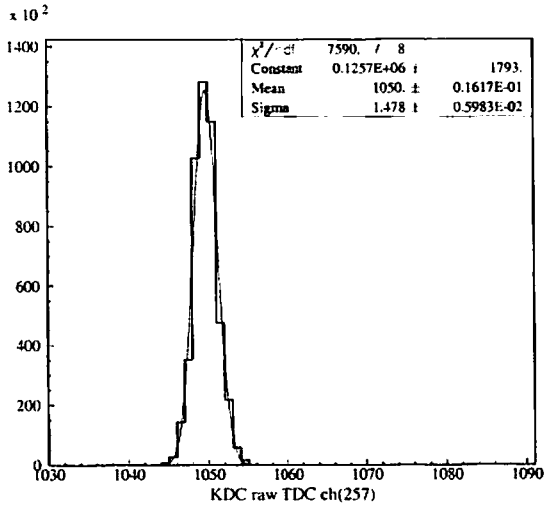

Figure 2: A trigger time spectrum on long term stability test

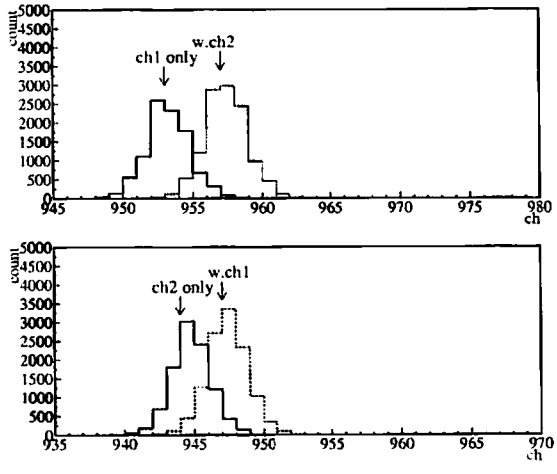

Figure 3: A trigger time spectrum in crosstalk test