N1 (GEP=3)

FPGA training course

Instructor: Koji Ishidoshiro (koji@awa.tohoku.ac.jp, RCNS Annex 221) and Koji Miwa (miwa9@lambda,phys.tohoku.ac.jp) GPPU Experimental Point (GEP): 3

Goal of Study

The students will learn basic of Field-Programmable Gate Array (FPGA) and Hardware Description Language (HDL) and obtain the methods to develop FPGA circuits using Xilinx Vivado. After this course, the students can start to develop FPGA circuits.

Contents

Field-Programmable Gate Array (FPGA) is one of key components for digital signal processing in the experiments of particle and nuclear physics. For the development of FPGA circuits, knowledge of digital circuits and implementation methods to FPGA is required. This course focus to introduce the latter experience.

In this course, we will use Xilinx Artix-7 FPGA with Vivado. The students are expected to install Vivado on their computers before the course. We do not recommend to use virtual machine.

FPGA training course (2016)

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Textbook and References

[1] Textbook: http://openit.kek.jp/training/2016/fpga/docs/OpenIt_FTC_preparation.pdf
[2] Reference: http://openit.kek.jp/training/2016/fpga/docs/OFTC_ref_note.pdf
The latest version will be announced.

Progress Schedule

- ✧ Day 1
  - Lecture on digital circuit
  - Lecture on combinational circuit
- ✧ Day 2
  - Lecture on FPGA
  - Lecture on sequential circuit

Other Details

Course Period	Nov 2026
Place	Research Center for Neutrino Science Annex, 224
Number of Students	Max 5
Evaluation method	Report (100%)

In Addition

This course will be held with online style if the on-site lecture would not be allowed due to the COVID-19.
In this case, laptop PC and FPGA board will be lent to students and the course is open only for formal GP-PU students (M2 students are not included).