

# ILC バーテックス検出器に向けた SOI ピクセルセンサーの開発研究

Development of SOI pixel sensors for the  
ILC vertex detector

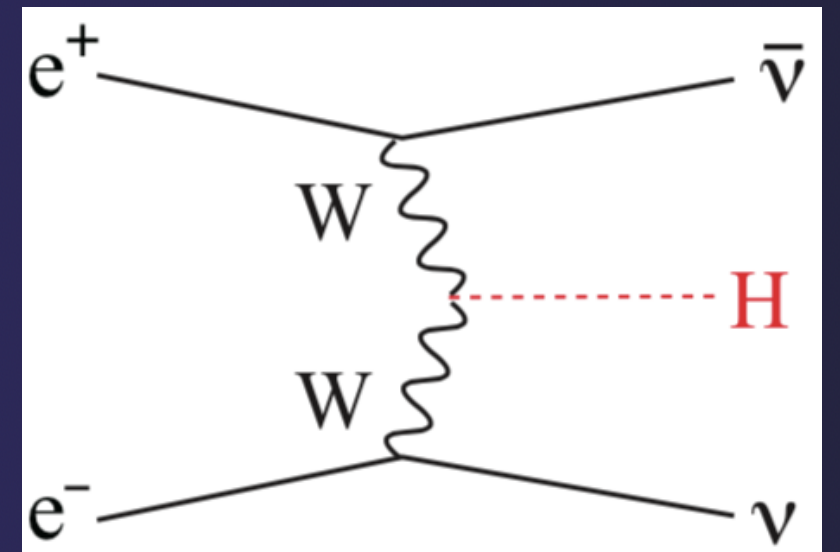
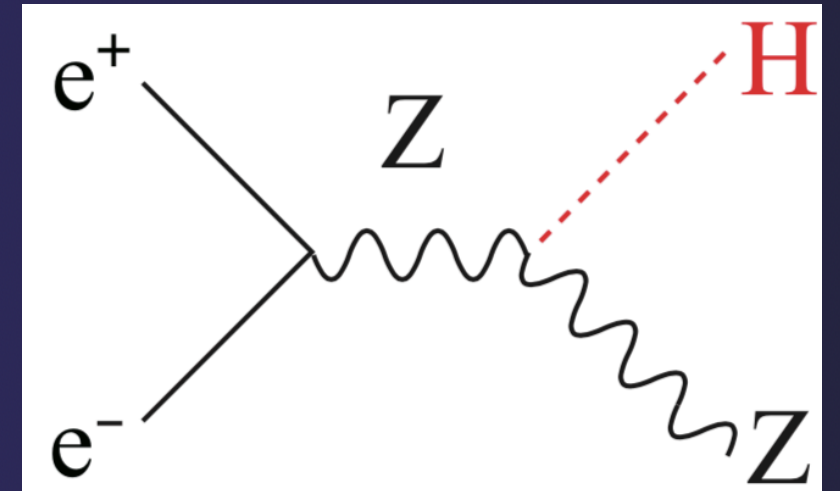
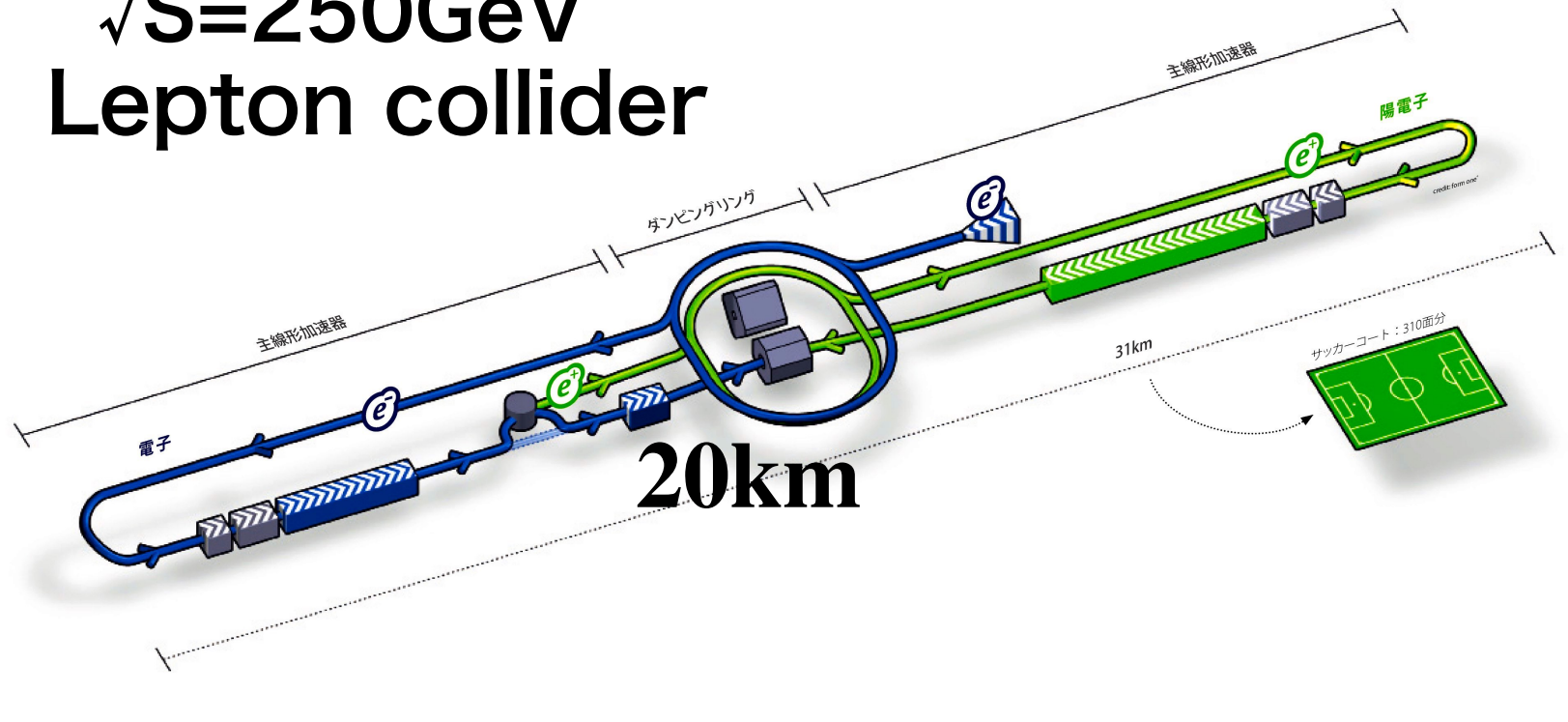


加速器科学研究室  
李 韜瀚

M2

# ILC(International linear collider)

$\sqrt{S}=250\text{GeV}$   
Lepton collider

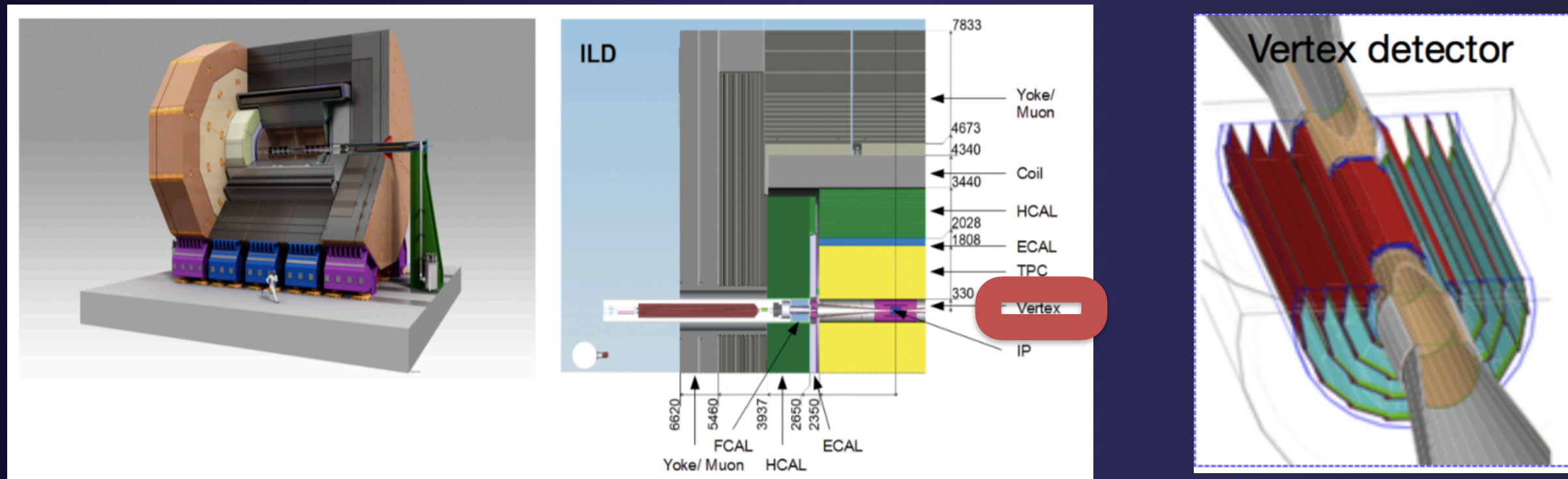


precision measurements of Higgs couplings

Motivation : for searching new physics.



# ILD(International Large Detector)



## Vertex :

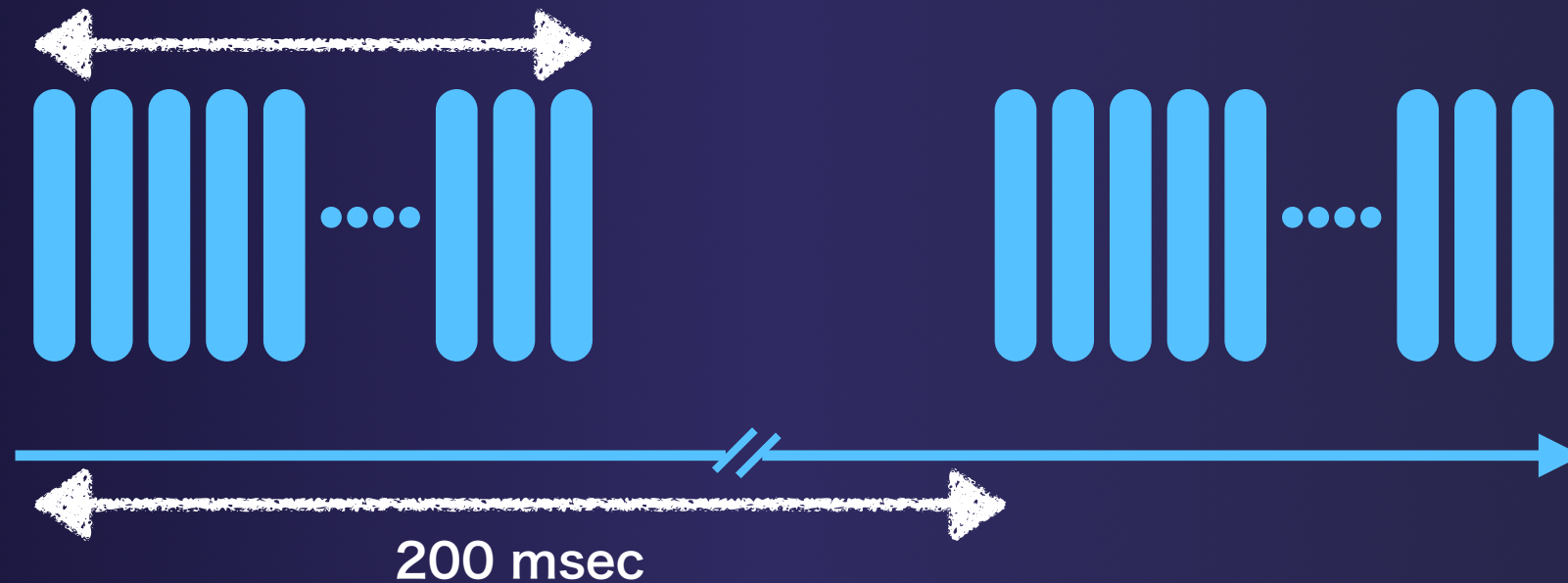
The identification of heavy quarks and tau leptons is essential for the ILC.

The reconstruction of decay vertices of long lived particles, such as D or B mesons, deserves therefore much attention and requires a particularly light and precise vertex detector.



# Vertex detector for ILC (International Linear Collider)

~1300 beam bunches (every 554 nsec)



## Requirement :

time resolution 554 nsec for specifying the bunch which has hit.

Spatial resolution 3  $\mu\text{m}$  for reconstruct the interaction point.

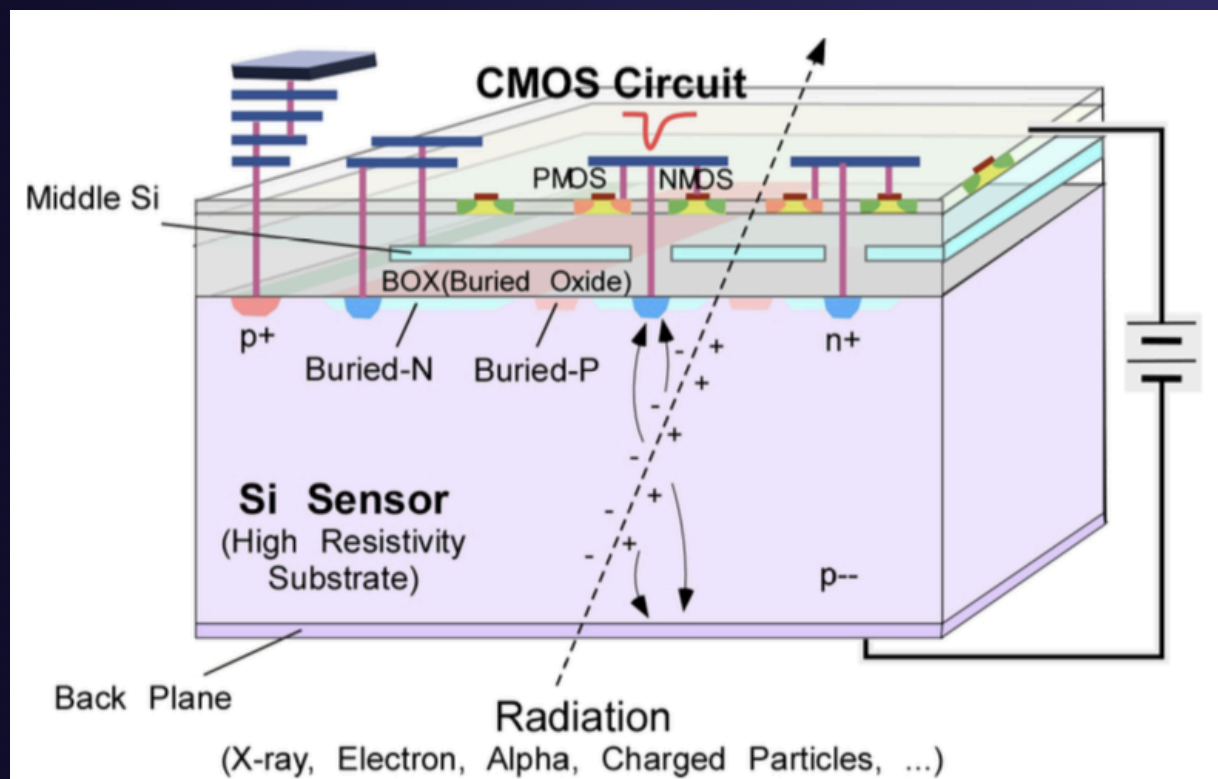
Low material budget for lepton collider.

A pixel occupancy not exceeding a few %

Etc.

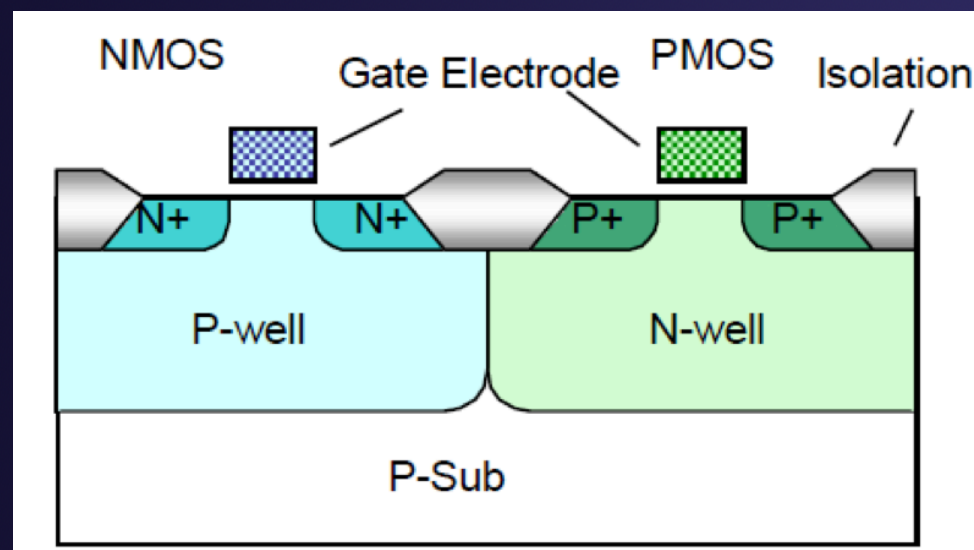


# SOI pixel detector

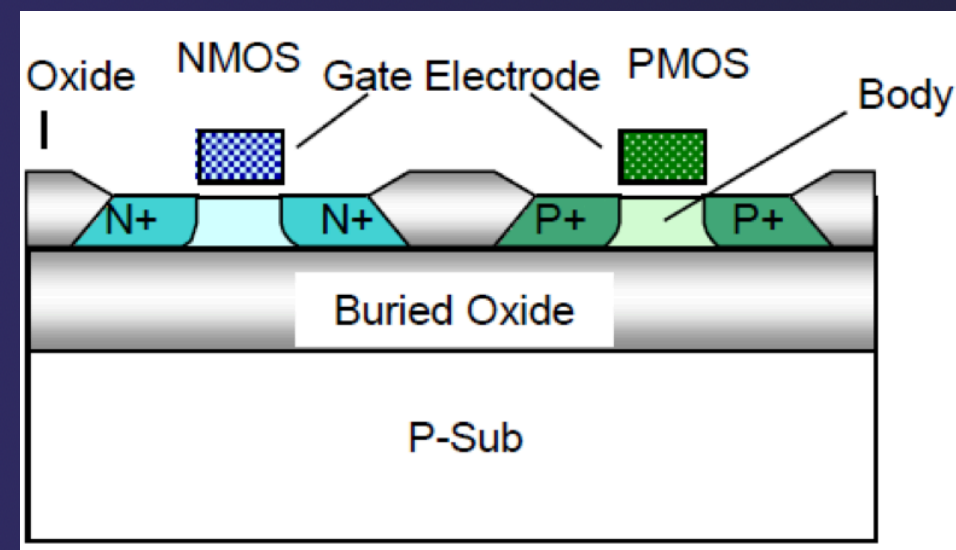


## Monolithic pixel sensor

- CMOS circuit
- BOX (Buried Oxide)
- Si sensor (Full depletion)



Bulk CMOS



SOI

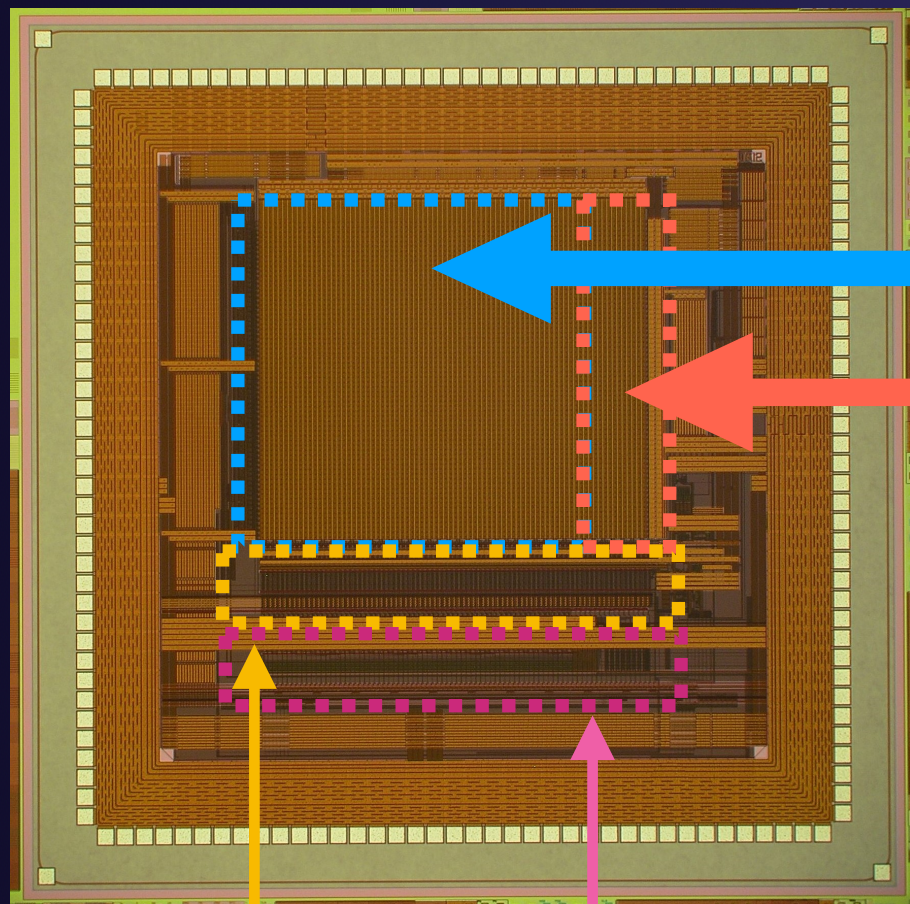
SOI sensor can make a full depletion layer .



# SOI detector designed for ILC vertex detector

Specification of SOFIST ver.2

Item	Specification
timestamp pixel	64×64
Analog signal pixel	16×64
Pixel size	25 μm×25 μm
Chip size	4.45mm×4.45mm
Chip thickness	75 μm



Column ADC

Zero-suppression logic

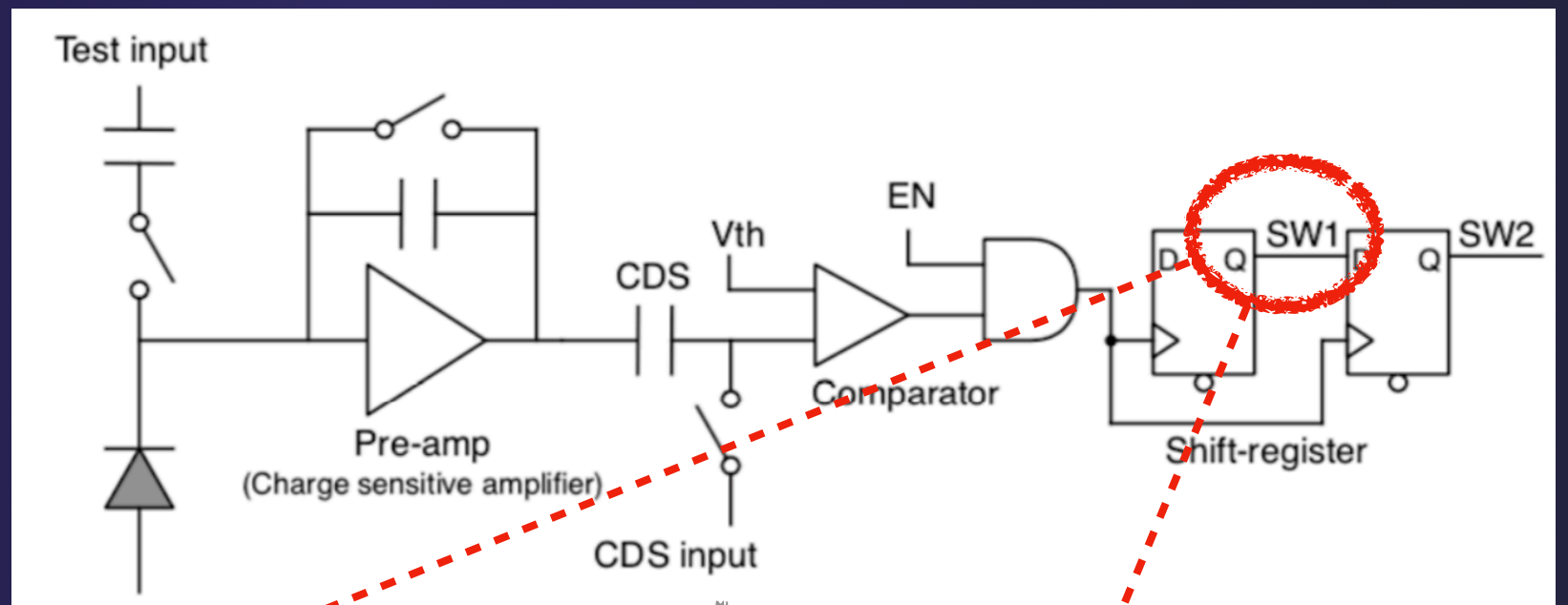
SOFIST ver.3 & ver.4 were designed that timestamp and analog signal are on one pixel.

In ver.2, timestamp and analog signal was designed on different pixels for identifying functions.

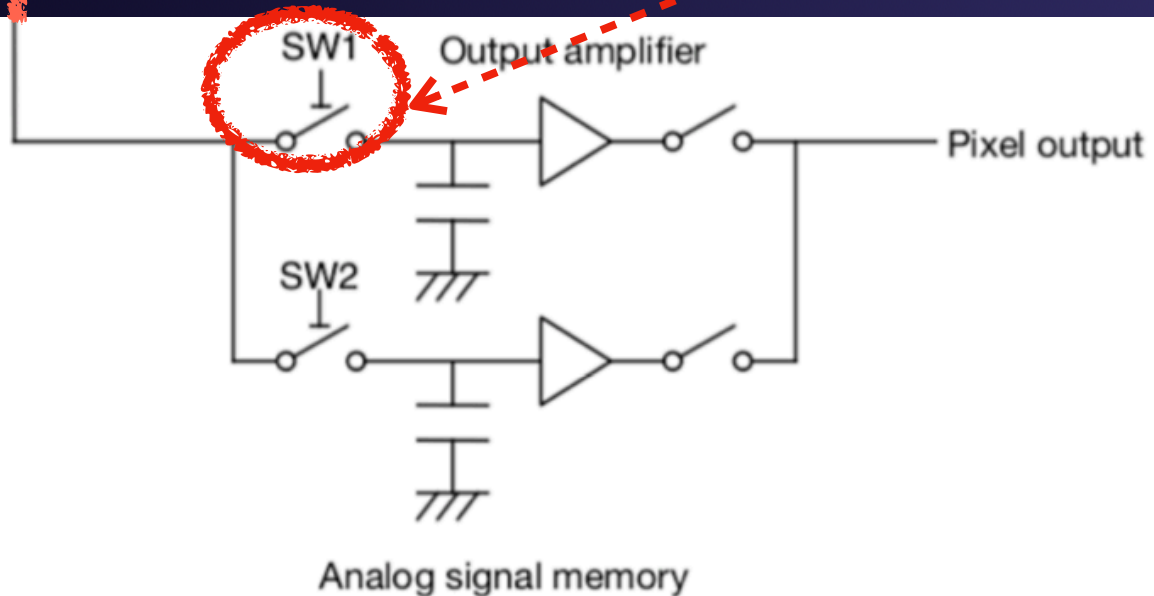


# Pixel circuit of SOFIST ver.2

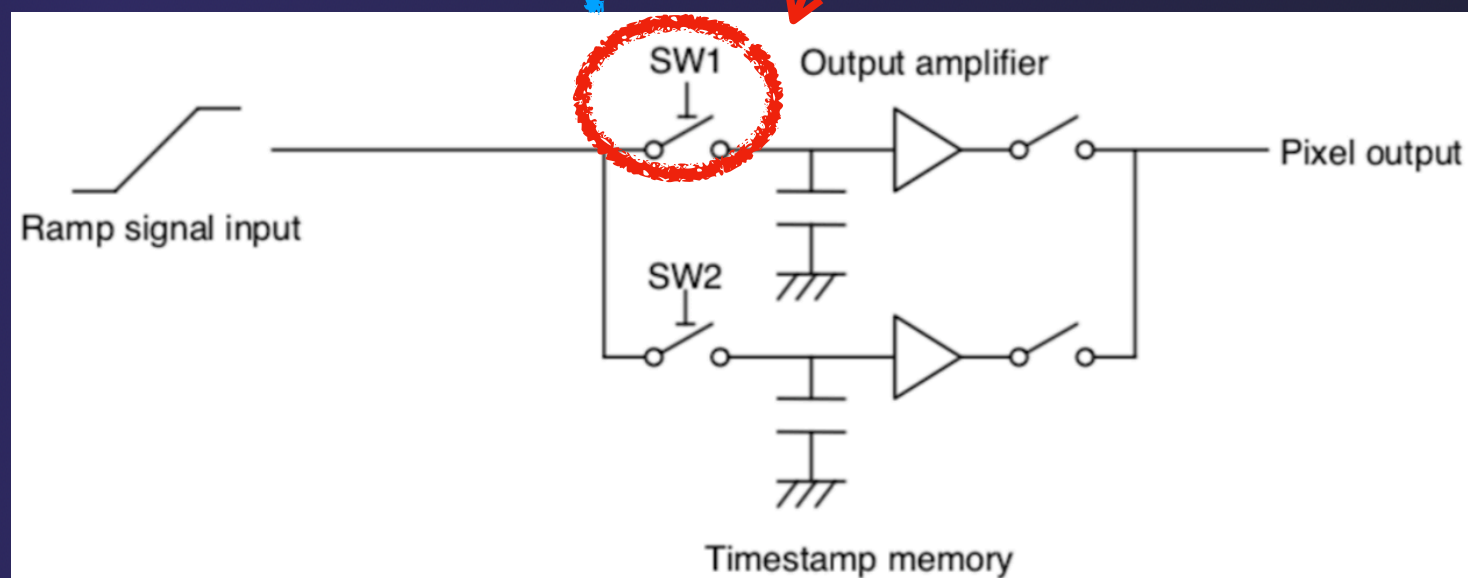
Charge signal is amplified by Pre-amp, then comparator has a threshold to identify whether it is a signal.



Analog



Time



In Analog signal memory pixel, charge signal will be output in analog .

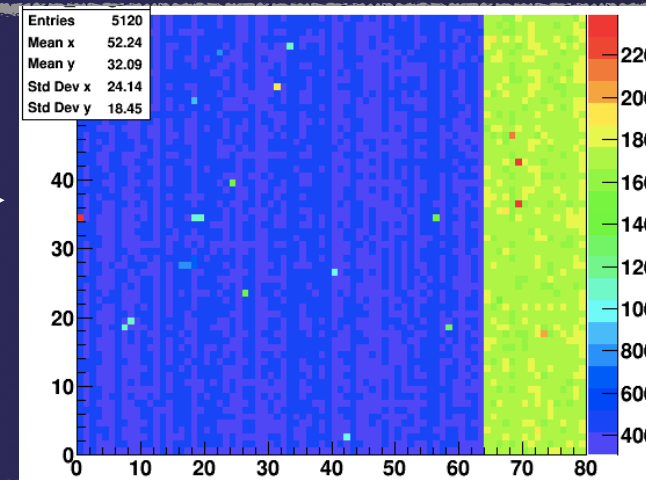
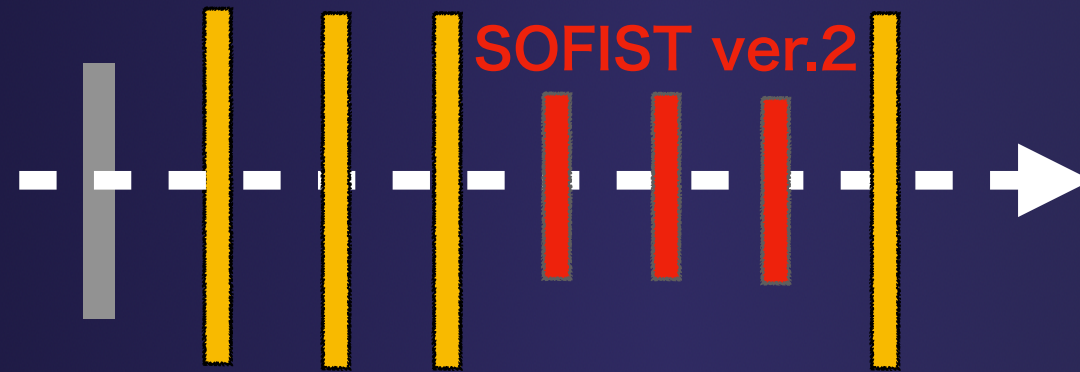
In timestamp memory, when comparator work, ramp voltage will be captured then to be output in analog.



# Evaluation method

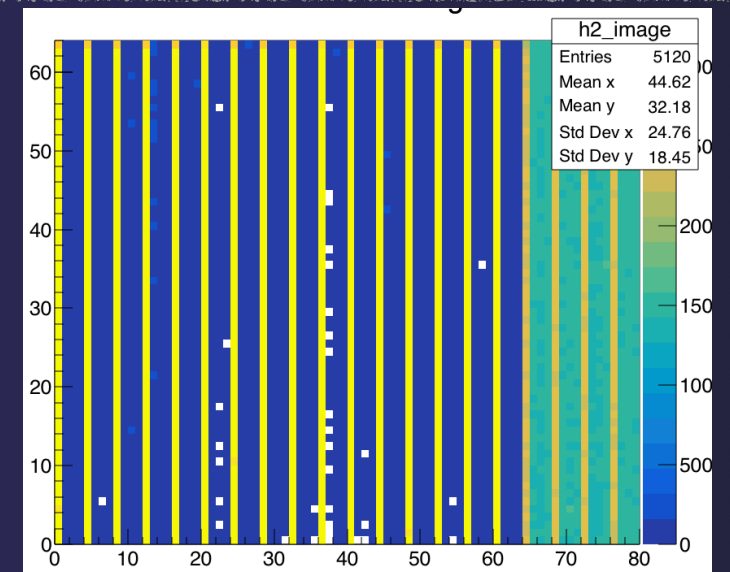
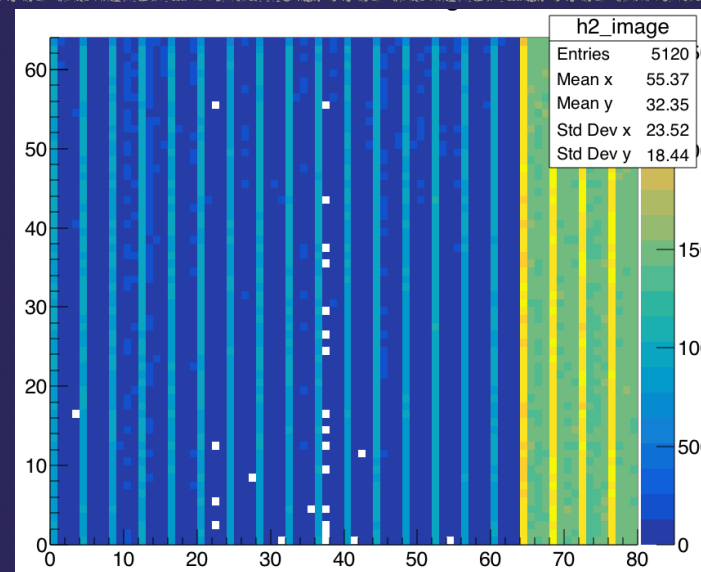
## Beam test

120 proton beam  
@Fermilab



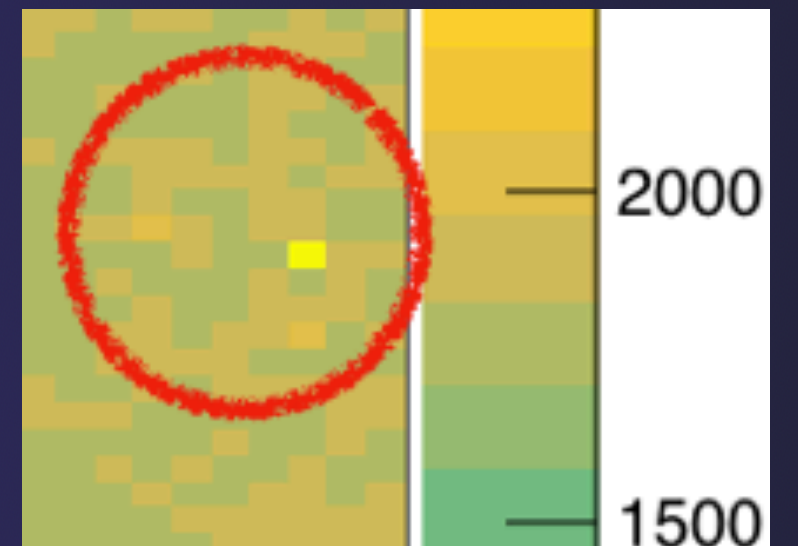
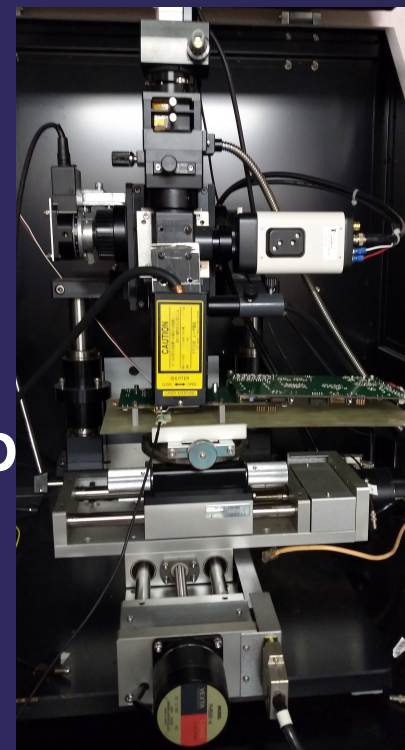
## Testpulse

- Pixel circuit test
- Test pulse is made by FPGA
- Time and voltage of test pulse can be controlled



## Infrared laser

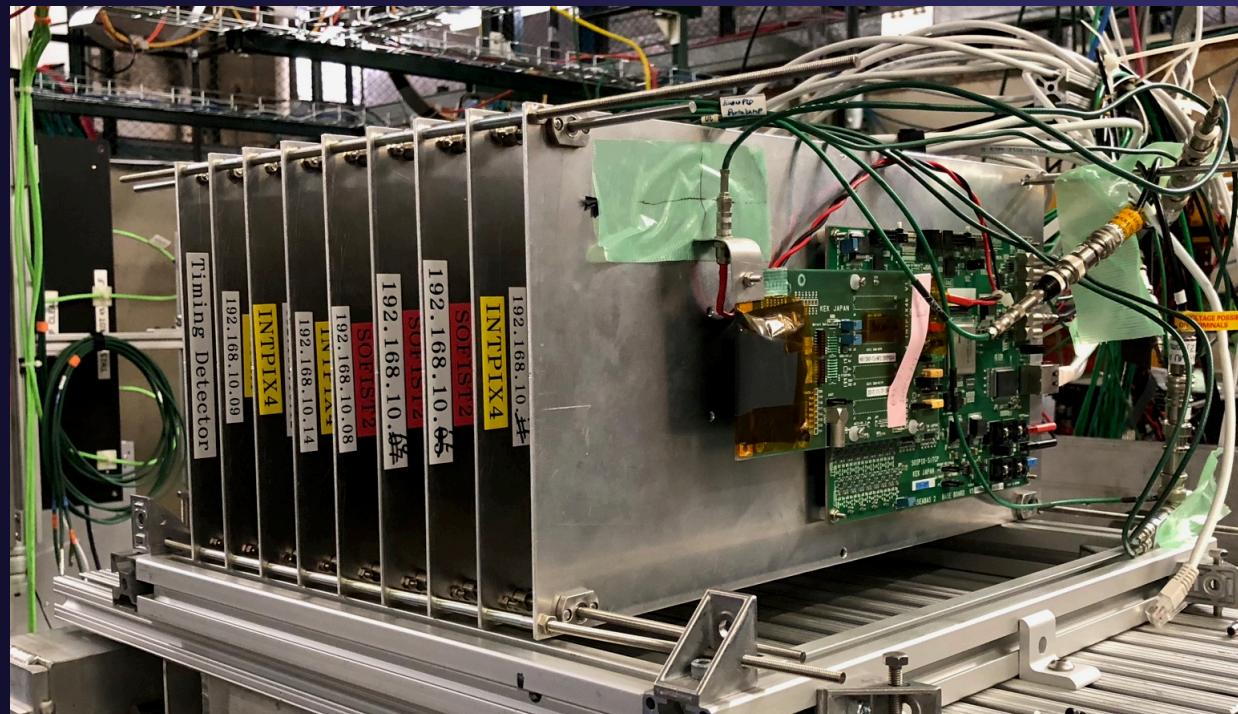
- Sensor test
- Infrared laser can go through SOFIST which has  $75 \mu\text{m}$  thickness
- @Tsukuba Uni. Particle experiment lab
- time and pixel address can be controlled



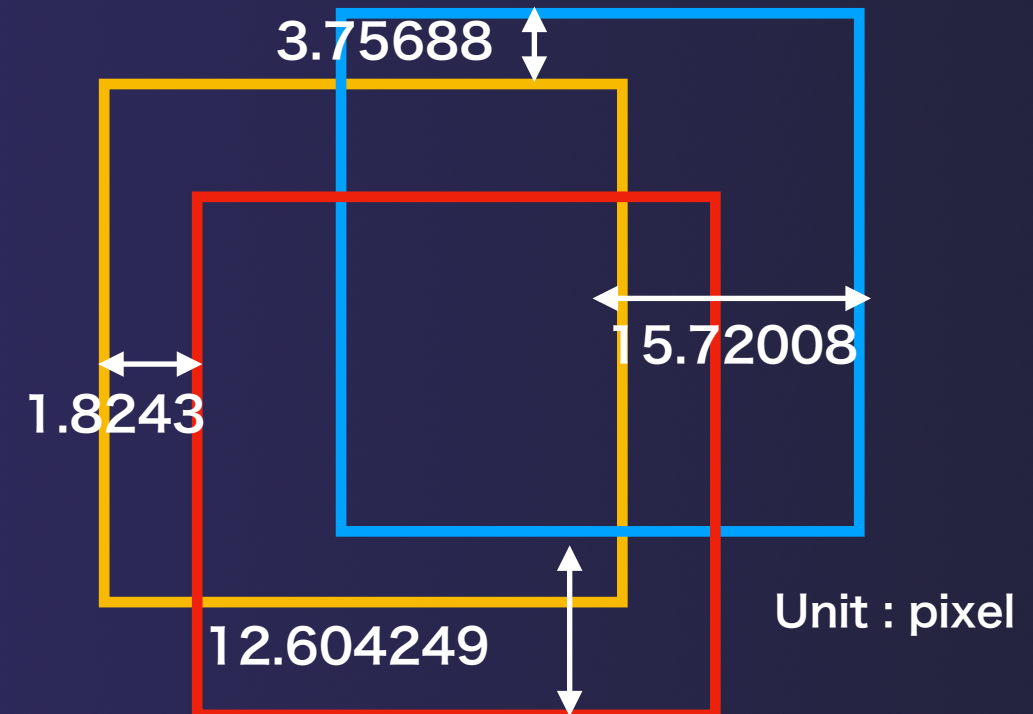


# Beam test

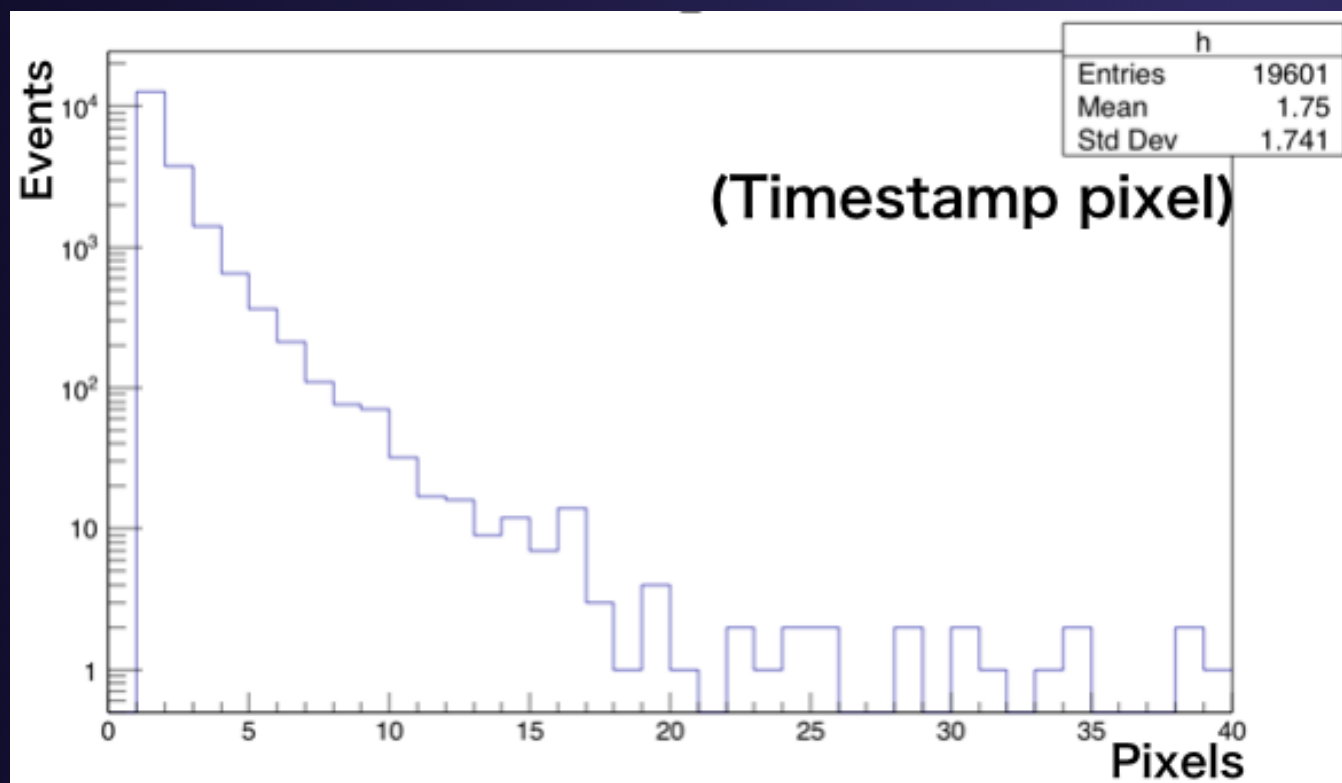
Photo of beam test set up in Fermilab



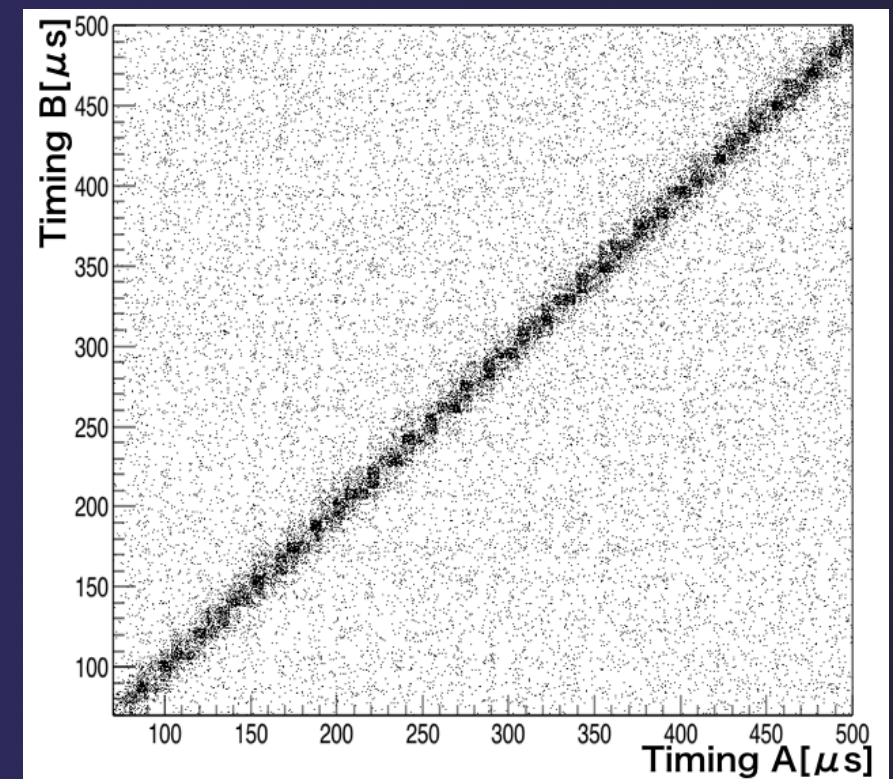
The relation of Chips' position



120 GeV protons were signals by 1 or 2 pixels on SOFIST2



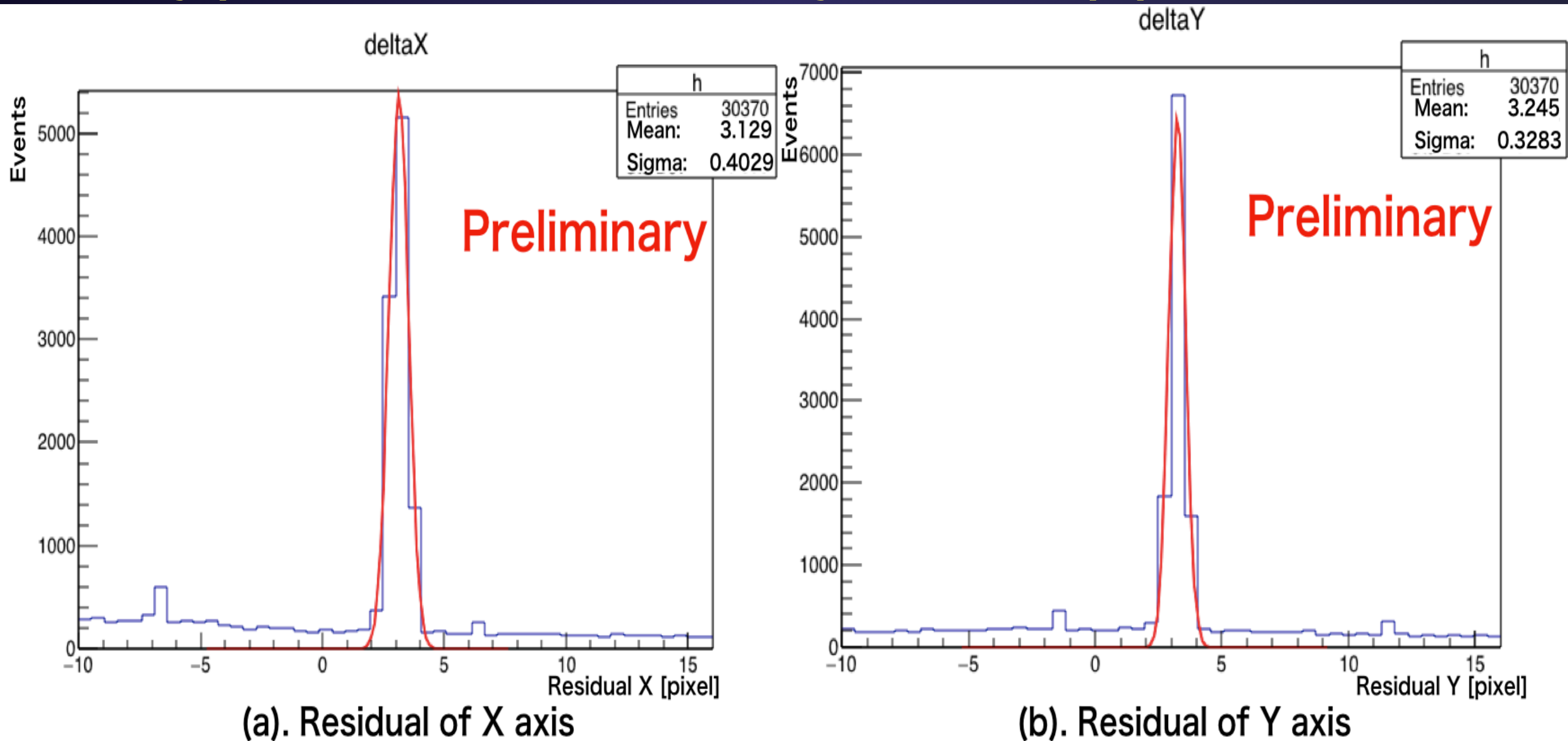
Time correlation of two sensors (protons)





# Position resolution of SOFIST ver.2 @120 GeV proton beam

## Binary position measurement by timestamp pixels



$\delta (X) : 8.4 \mu\text{m}$

$\delta (Y) : 6.7 \mu\text{m}$



# Time resolution of SOFIST ver.2

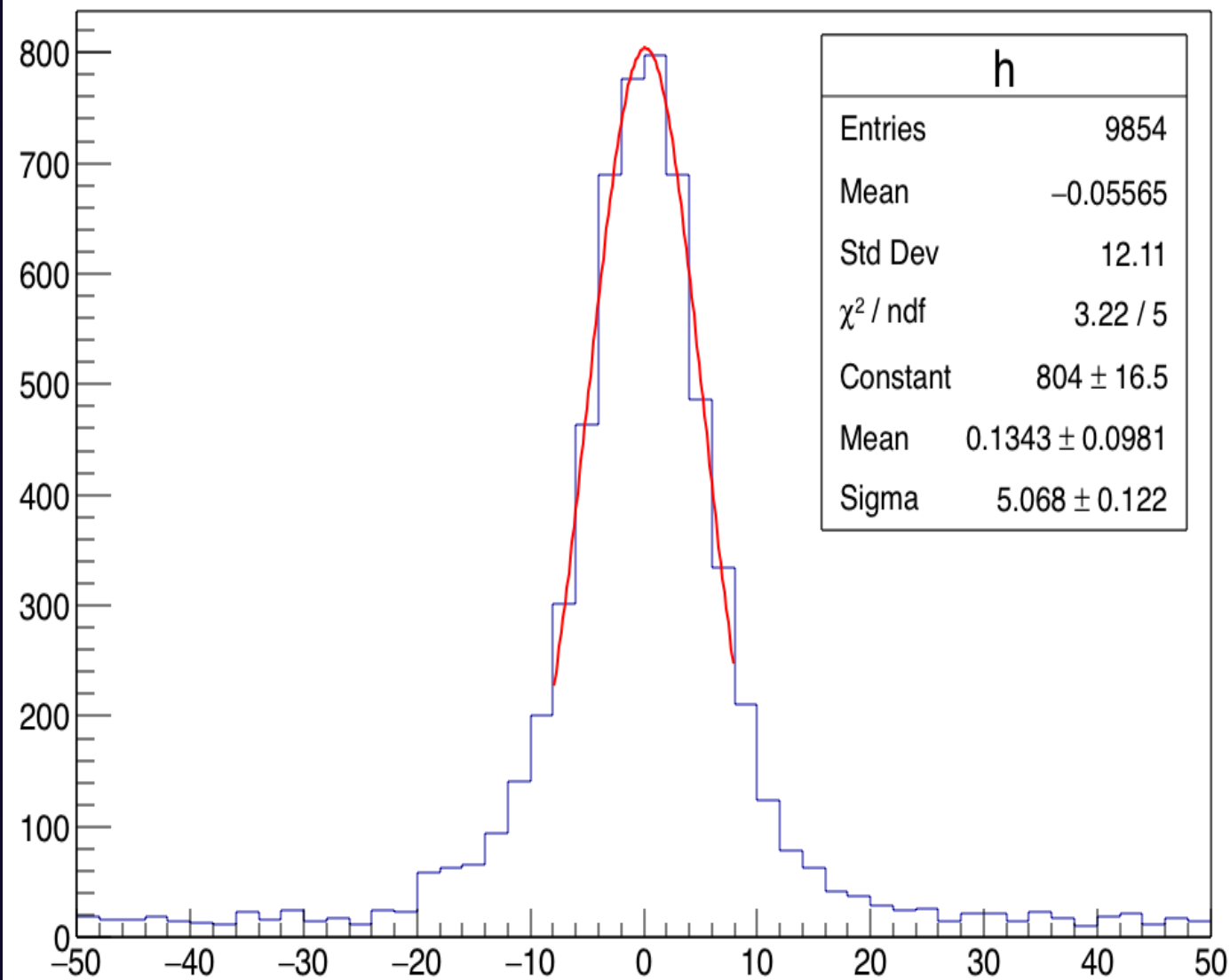
@120 GeV proton beam

@infrared laser

Time resolution Result of beam test

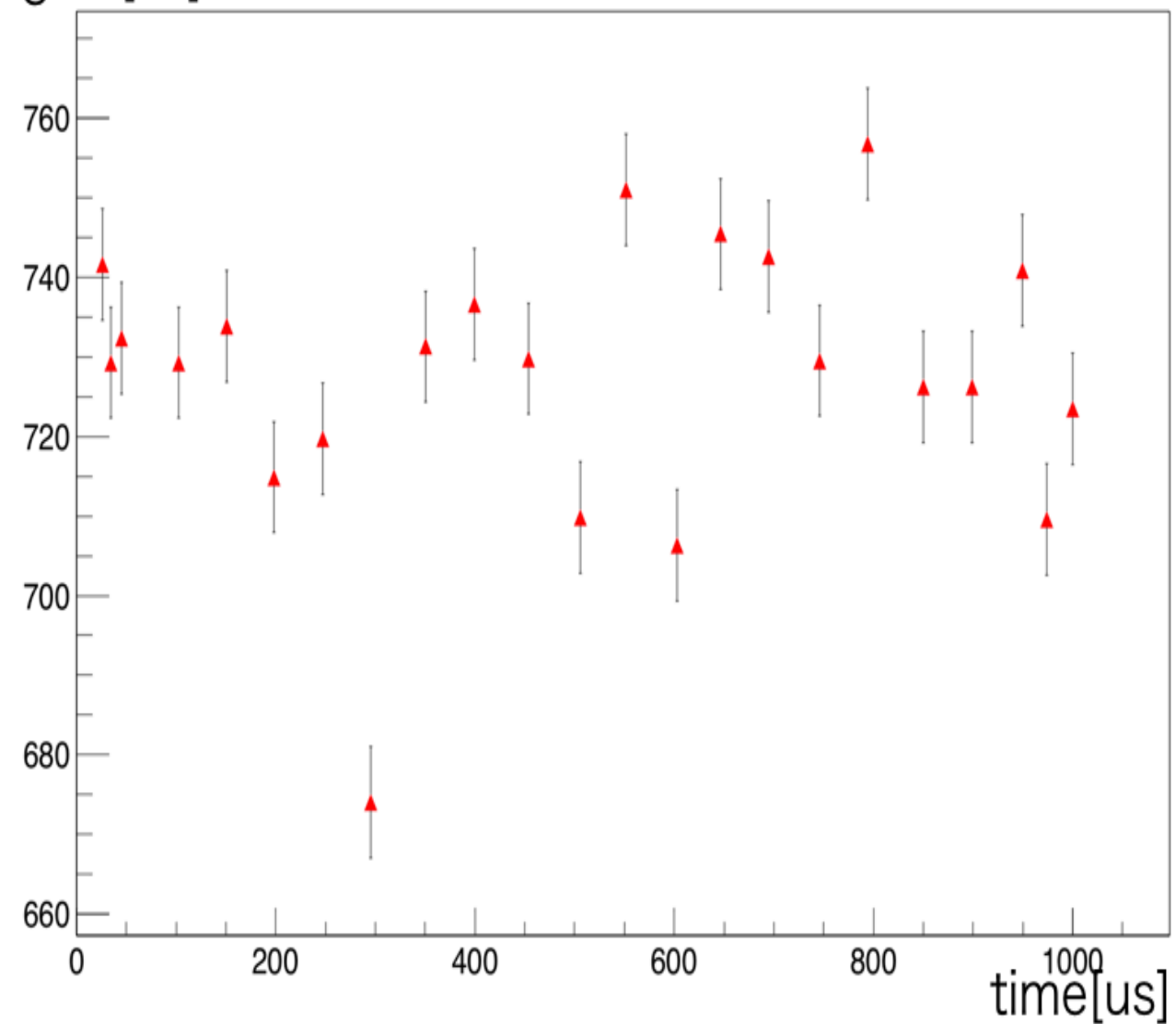
Time resolution by laser

time\_resolution



Time resolution  $5.68/\sqrt{2} = 3.58$  [ $\mu\text{s}$ ]

sigma[ns]

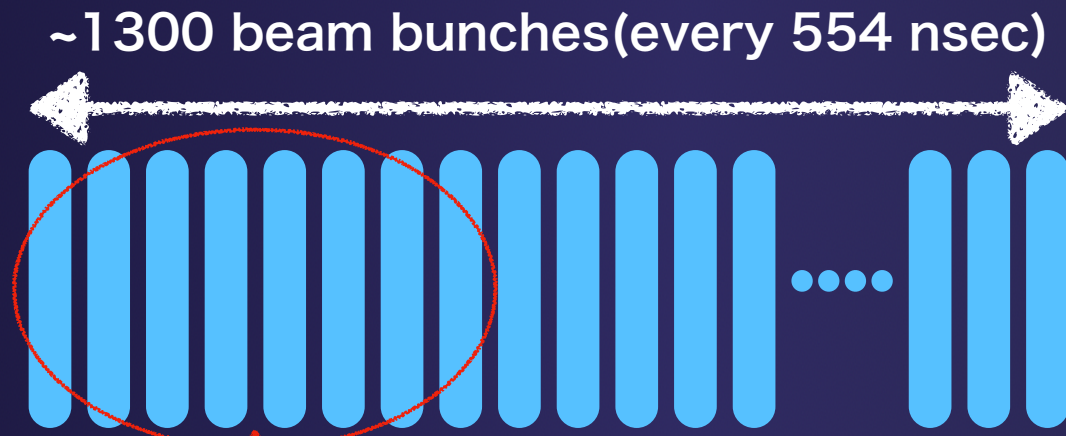


Time resolution  $\sim 730$  ns



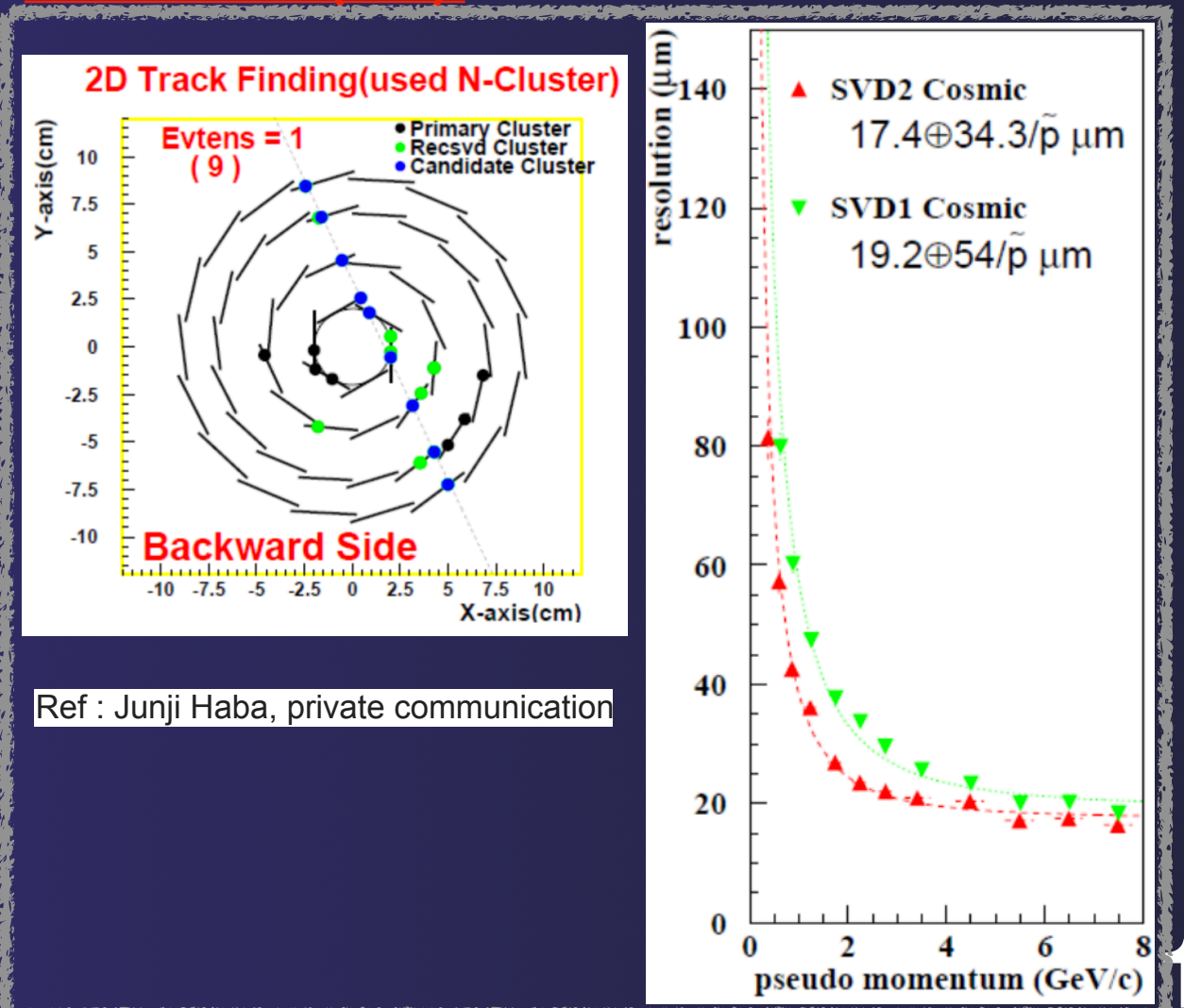
# Time resolution of SOFIST ver.2

Conclusion (Is 730 nsec good?):



730 ns time resolution can identify hit with 8 bunches ( $6\sigma$ ).

$6.32$  [hits/cm<sup>2</sup>/BX]      ····· ILC hit rate  
 $\times 1.75$  [pixel/hits]      ····· Cluster size  
 $\times 25 \cdot 25$  [ $\mu\text{m}^2$ /pixel]      ····· pixel size  
 $\times 8$  [bunches]  
 $\times (100 \cdot 100$  [ $\mu\text{m}^2$ /pixel] /  $25 \cdot 25$  [ $\mu\text{m}^2$ /pixel] )  
 ····· sensing area  
 $\approx 5.06 \times 10^{-3}$  [pixels]  
 $\sim 0.5\%$

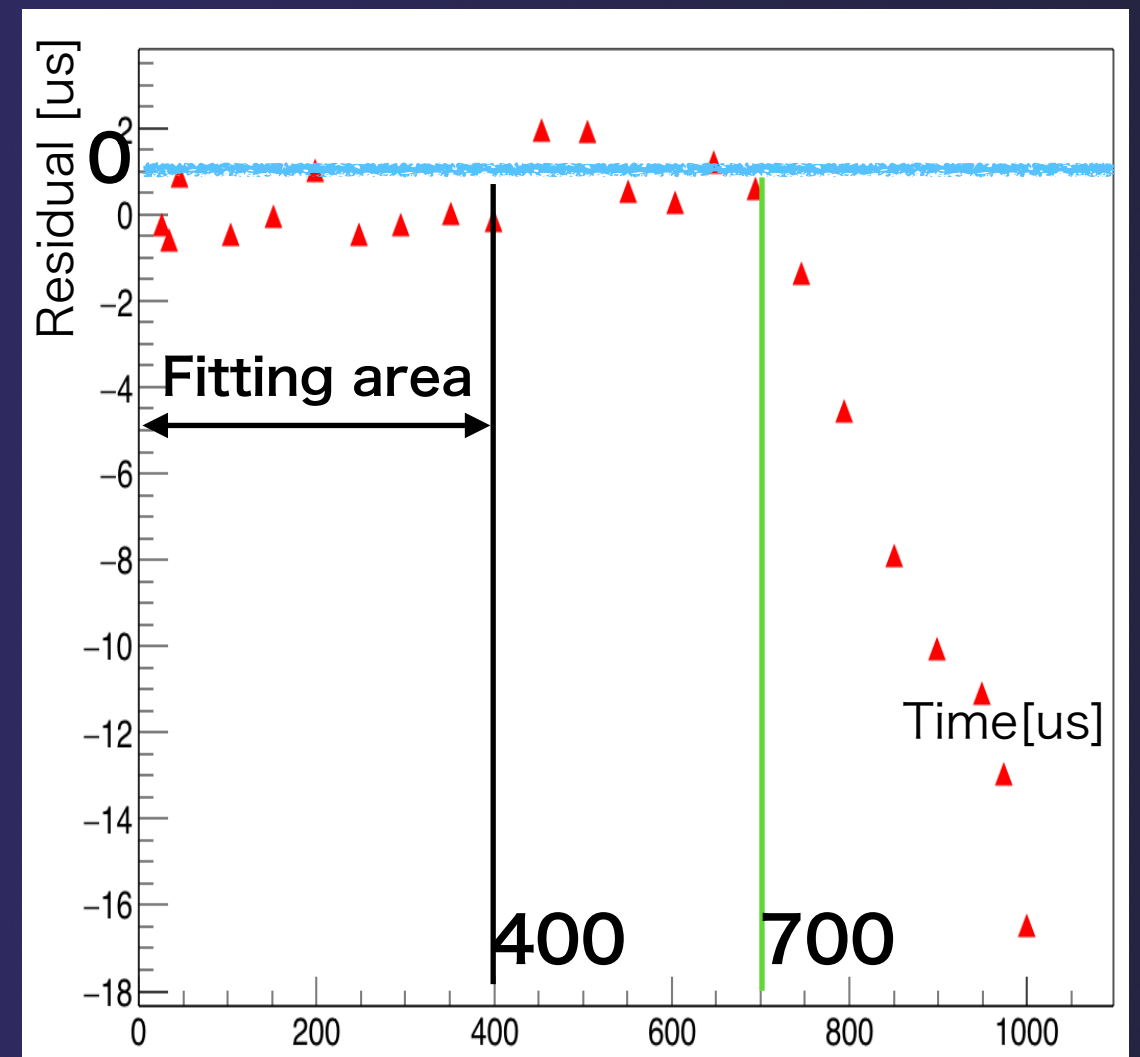
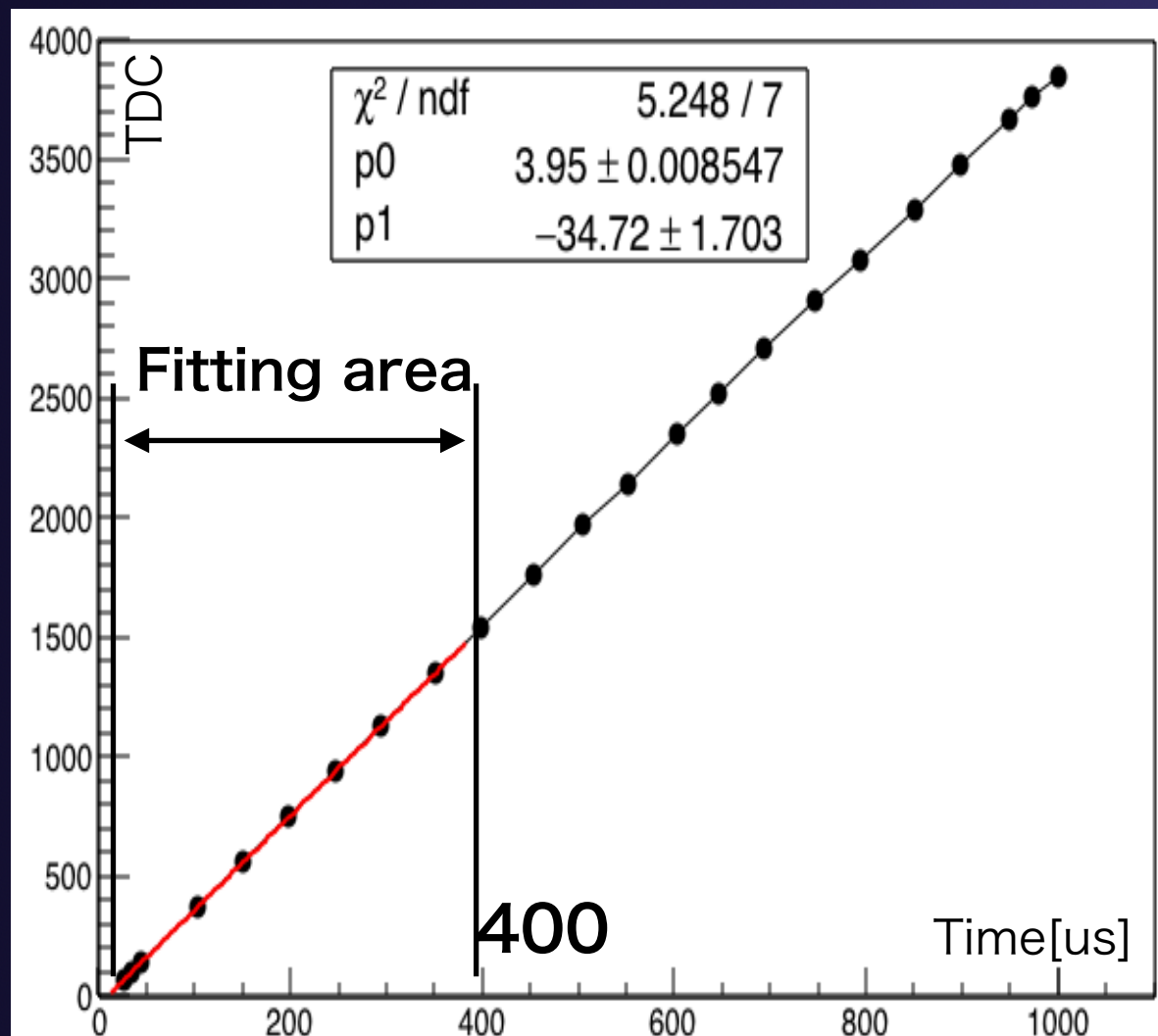




# Performance of Time measurement

## Linearity of time measurement

### @infrared laser



$$\text{TDC} = 3.96 \text{ time} - 36.02$$

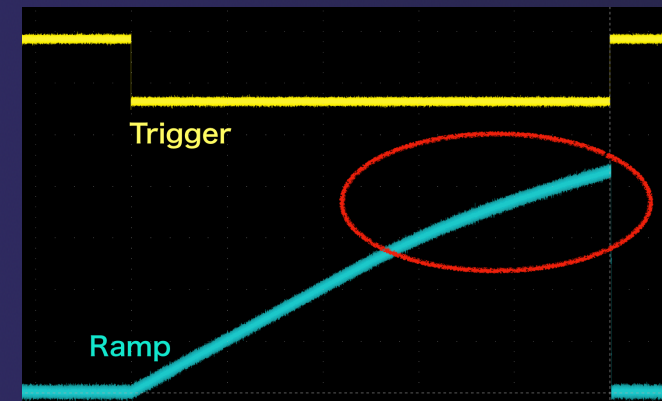


# Performance of Time measurement

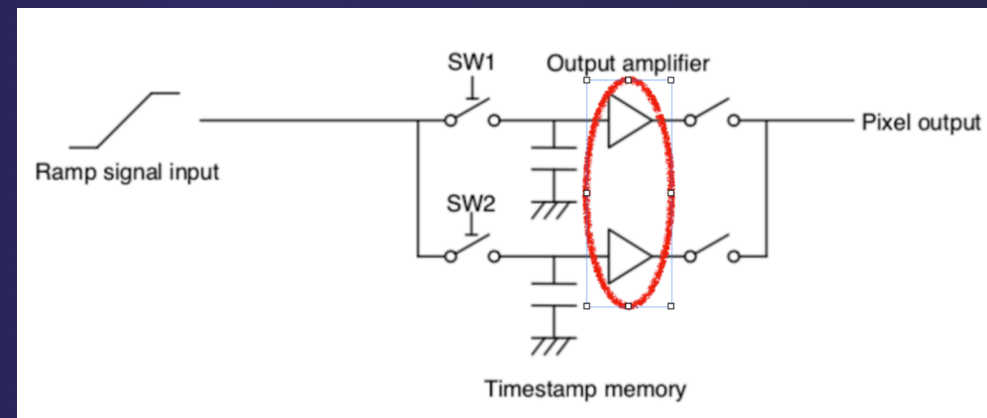
## Linearity of time measurement

### @testpulse

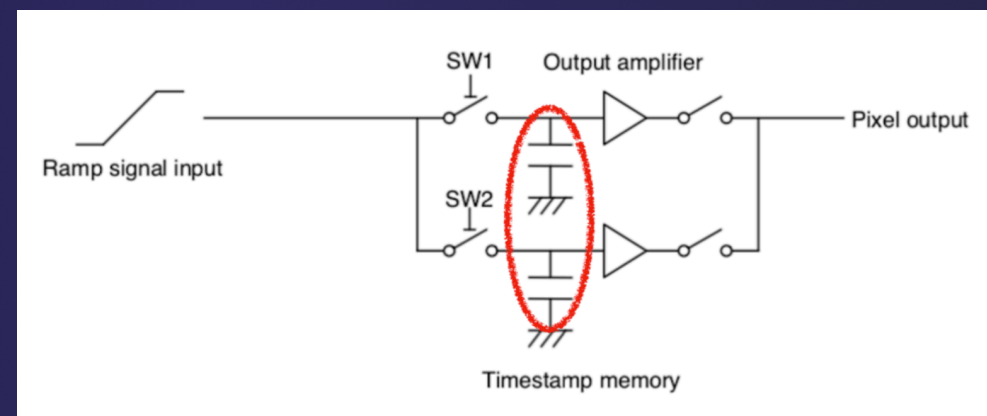
1. Ramp wave which is outputted from SEABAS board is not good ?



2. Gain of output amplifier become bad over 600 mV ?



3. Leak current from Capacitance affects output voltage ?



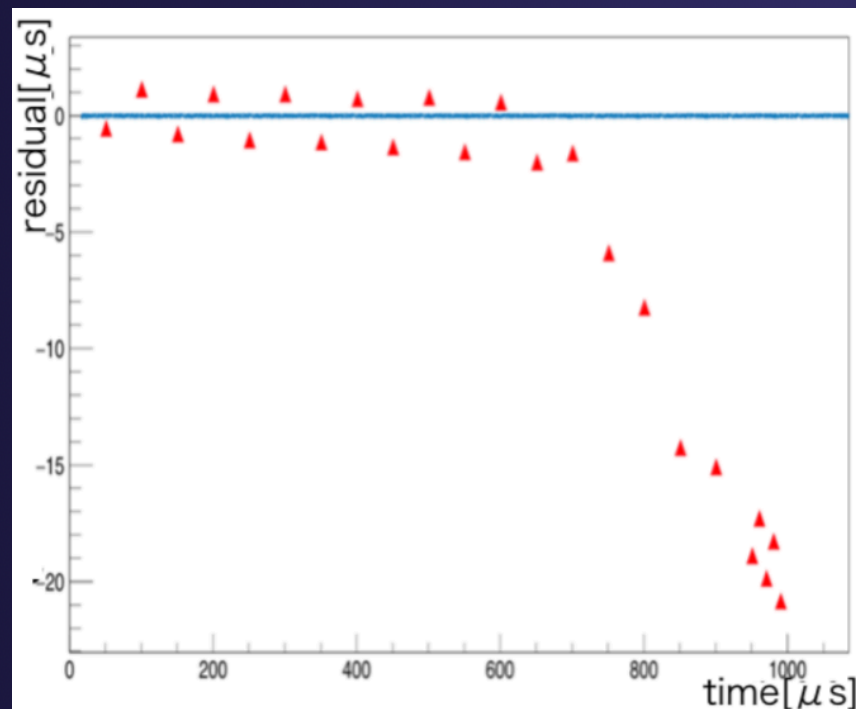
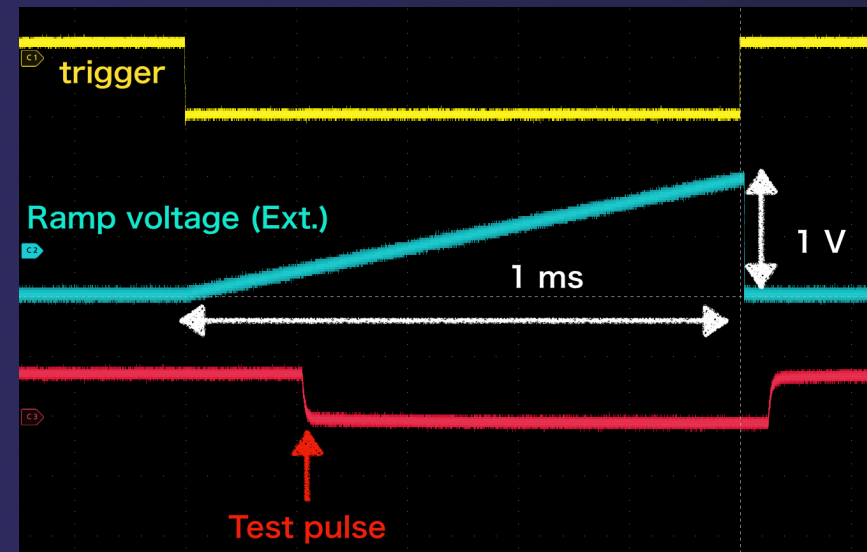
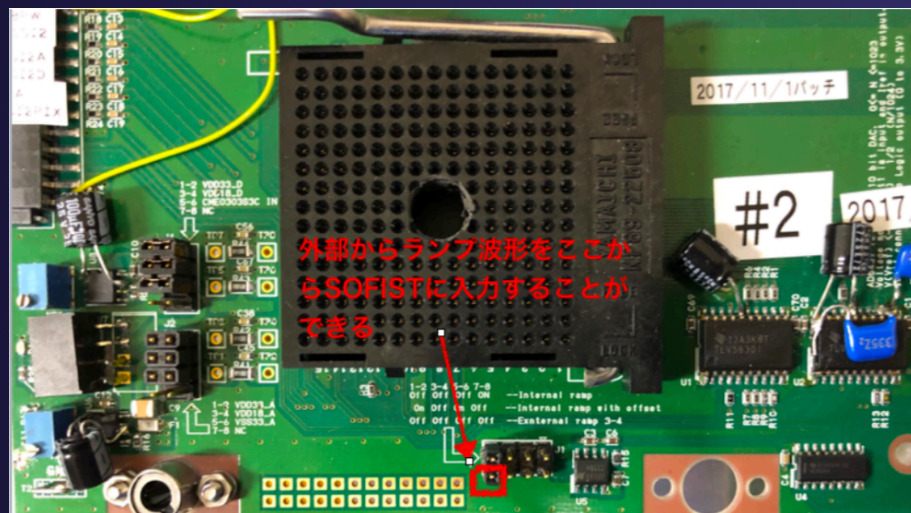


# Performance of Time measurement

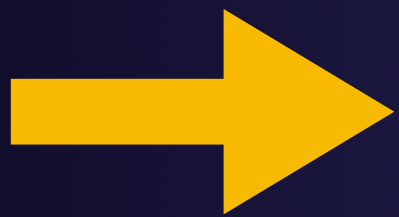
## Linearity of time measurement

@testpulse

1. Ramp wave which is outputted from SEABAS board is not good ?  
Solution : use ramp wave from function generator instead of board.



Result of residual of time measurement is same from ramp wave by board , so the reason is not from ramp wave.





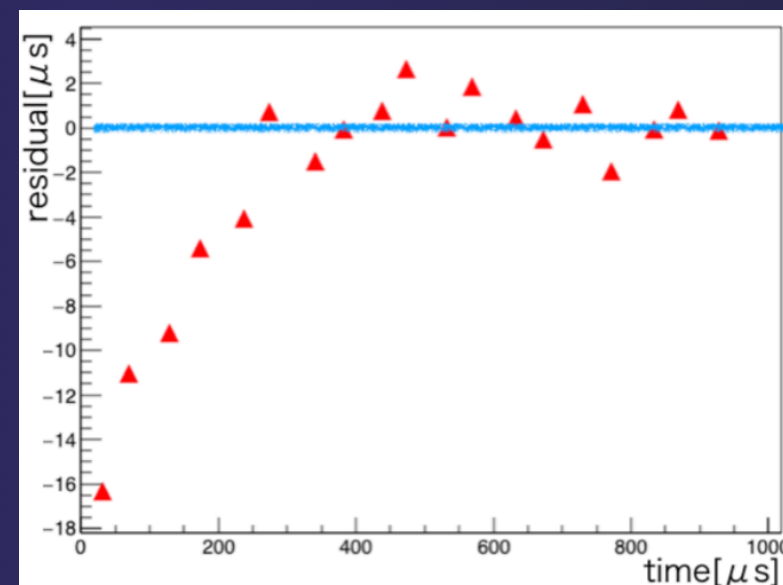
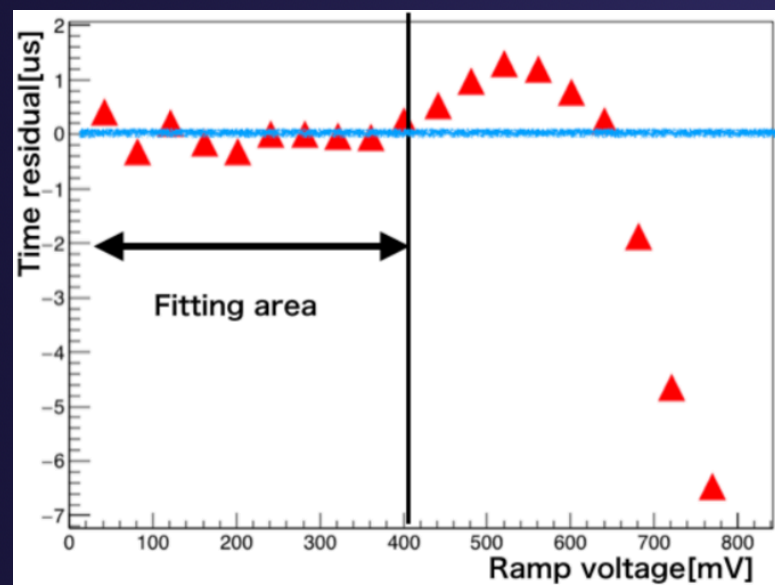
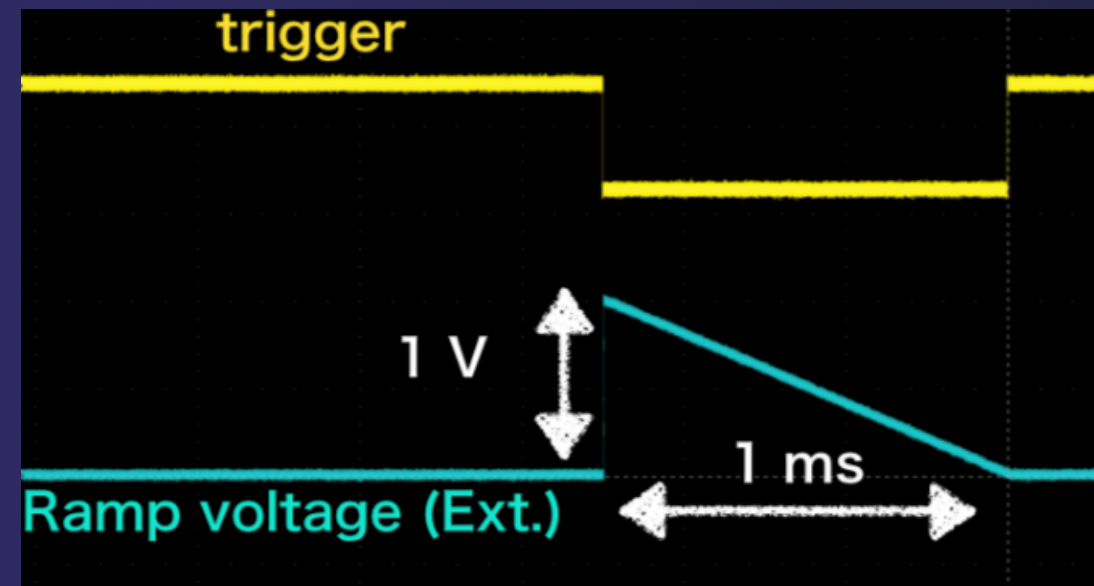
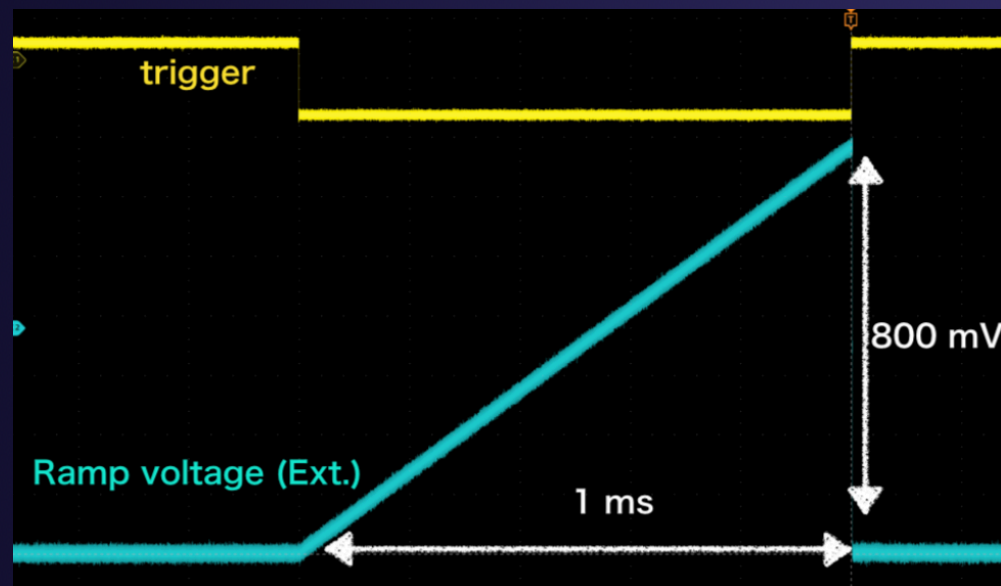
# Performance of Time measurement

## Linearity of time measurement

### @testpulse

2. Gain of output amplifier become bad over 600 mV ?

Solution : input low ramp voltage and ramp wave which has different form.



Gain of output amplifier become bad over 600 mV !!!



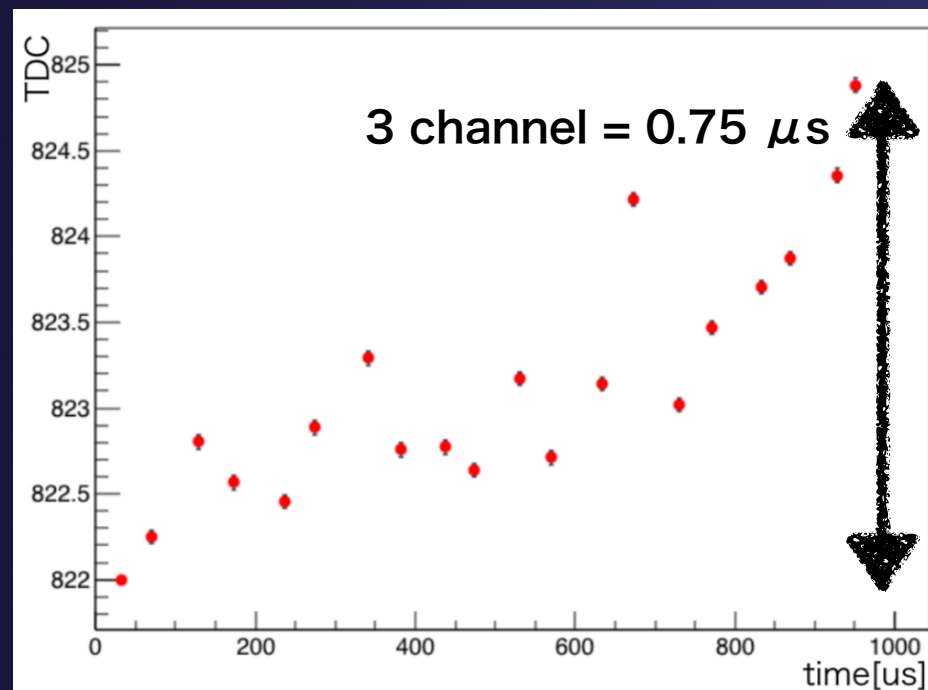
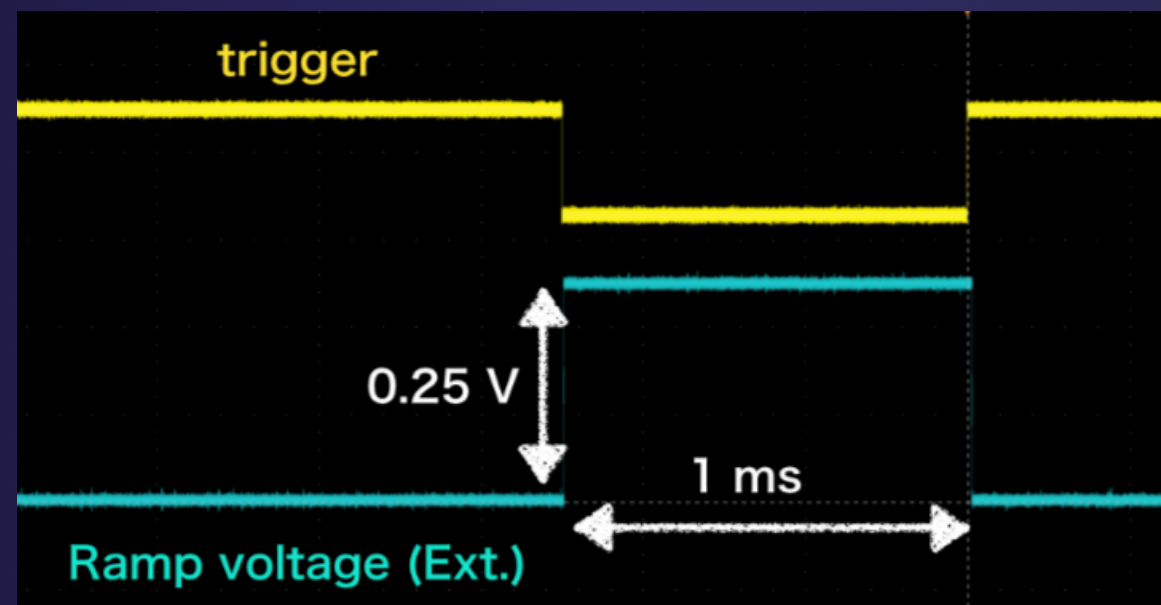
# Performance of Time measurement

## Linearity of time measurement

### @testpulse

3. Leak current from Capacitance affects output voltage ?

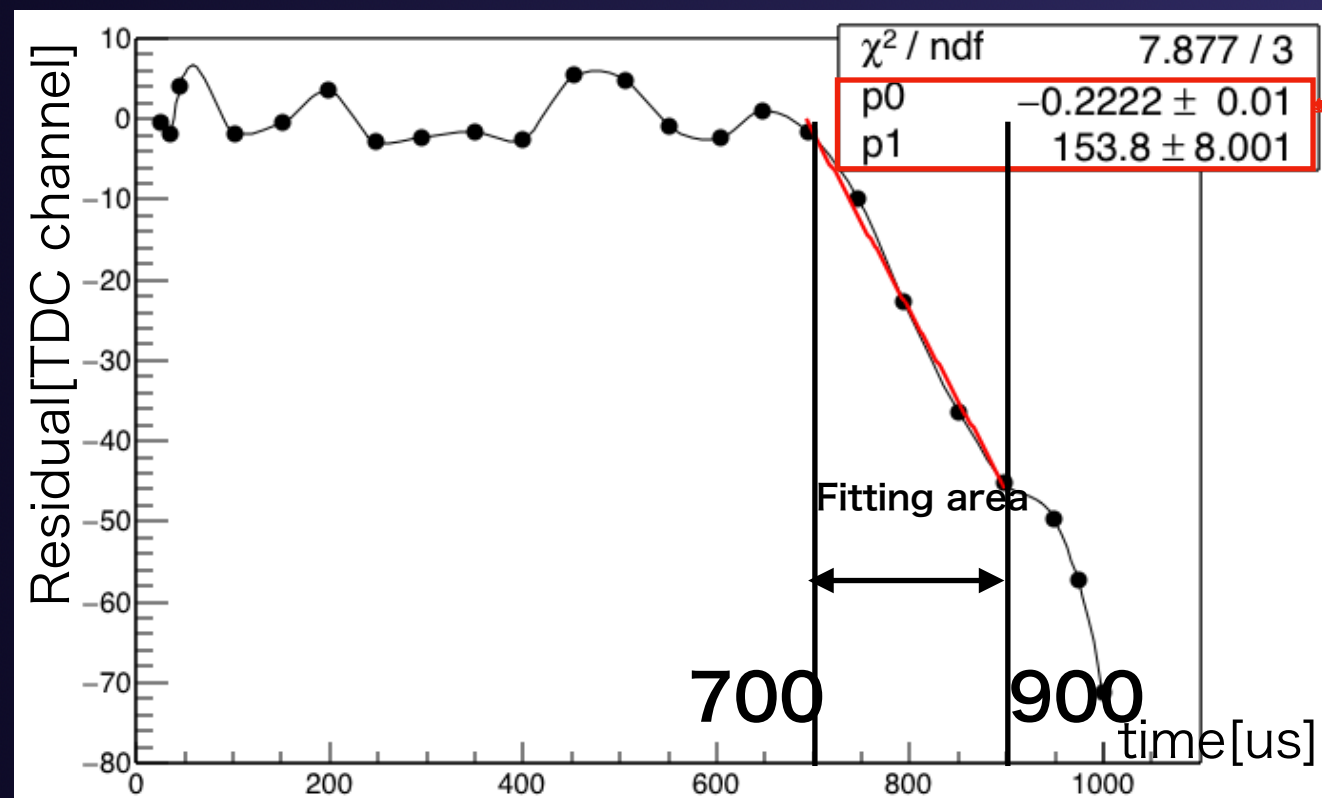
Solution : input square wave instead of ramp wave.



Capacitance leak current affects output voltage but just below  $0.75 \mu s$ .



# Performance of Time measurement



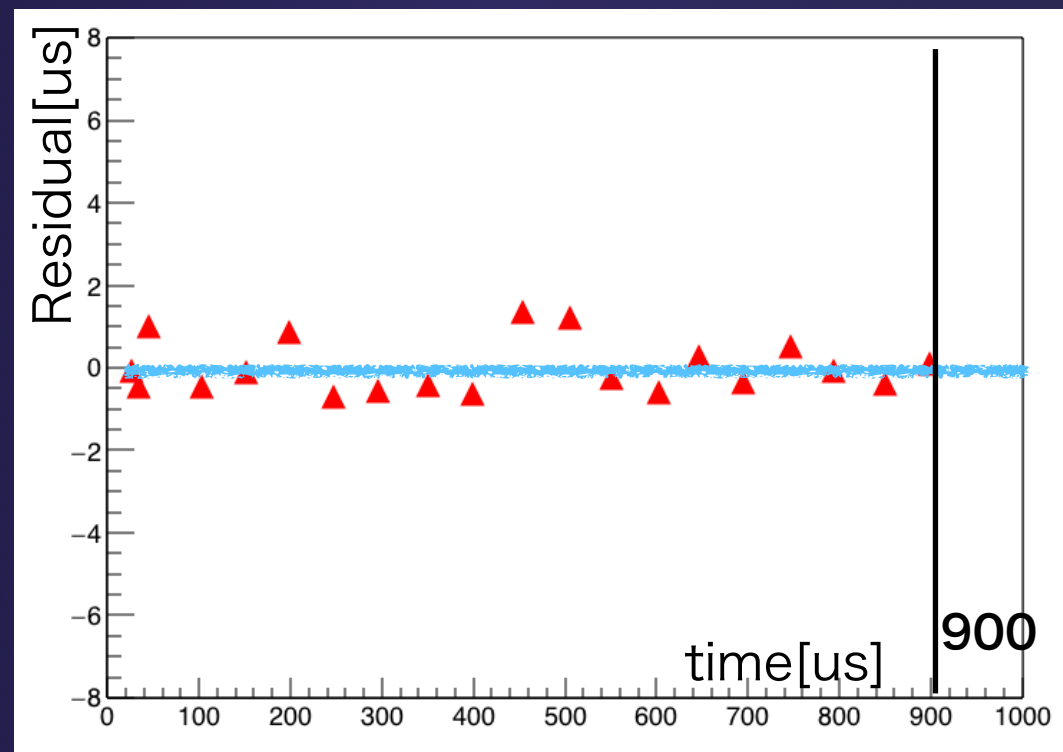
$\underline{\text{TDC}} = (3.957 + p0) \underline{\text{time}} - 35.49 + p1$   
 ( Parameter 3.957 and 35.49 are fitted from 0~700  $\mu\text{s}$ .)

(0~700  $\mu\text{s}$ )

$\underline{\text{TDC}} = 3.957 \underline{\text{time}} - 35.49 ;$

(700~900  $\mu\text{s}$ )

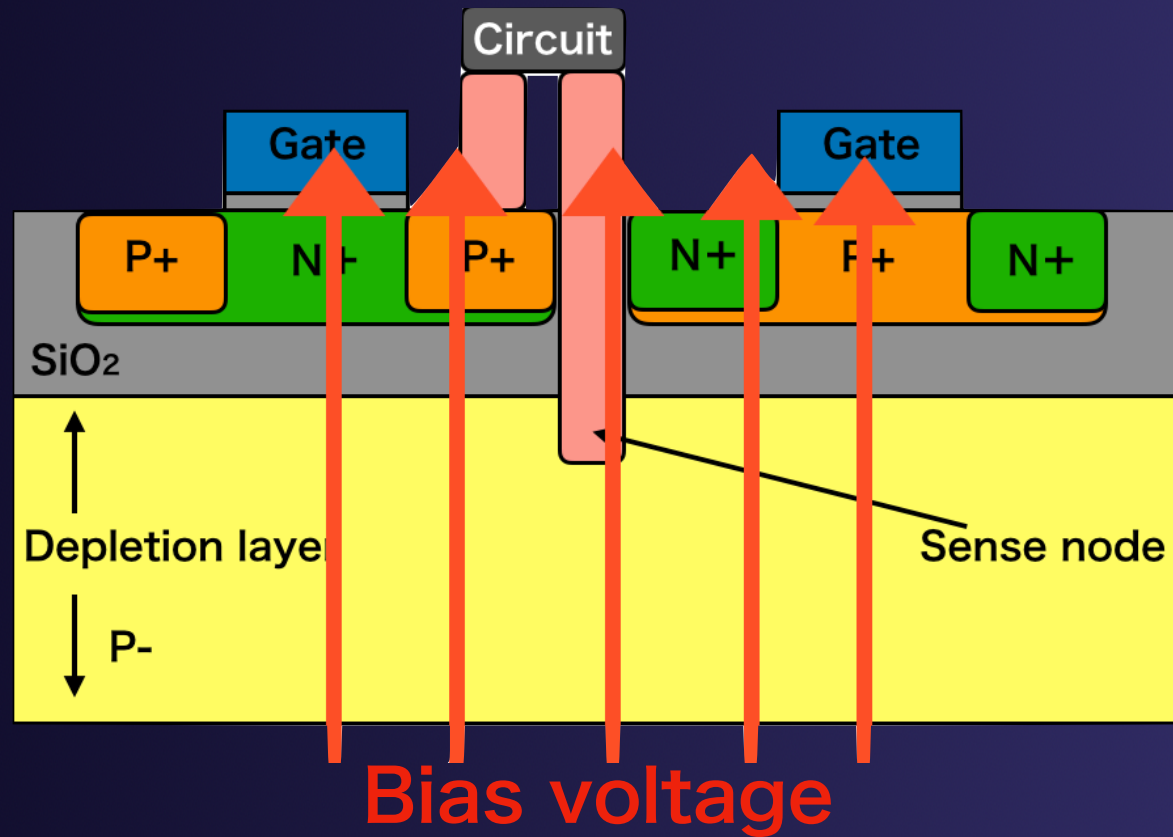
$\underline{\text{TDC}} = 3.735 \underline{\text{time}} + 118.31 .$



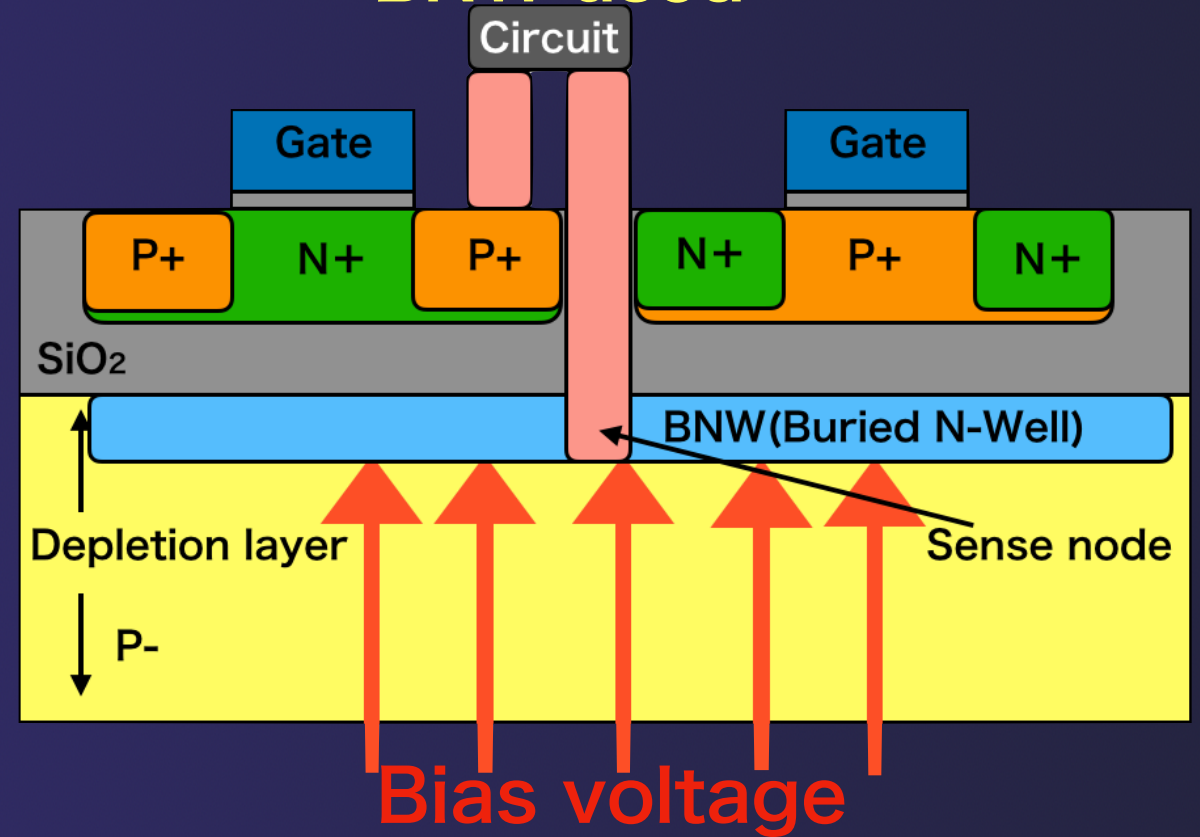


# BNW(Buried N-Well)

BNW didn't used



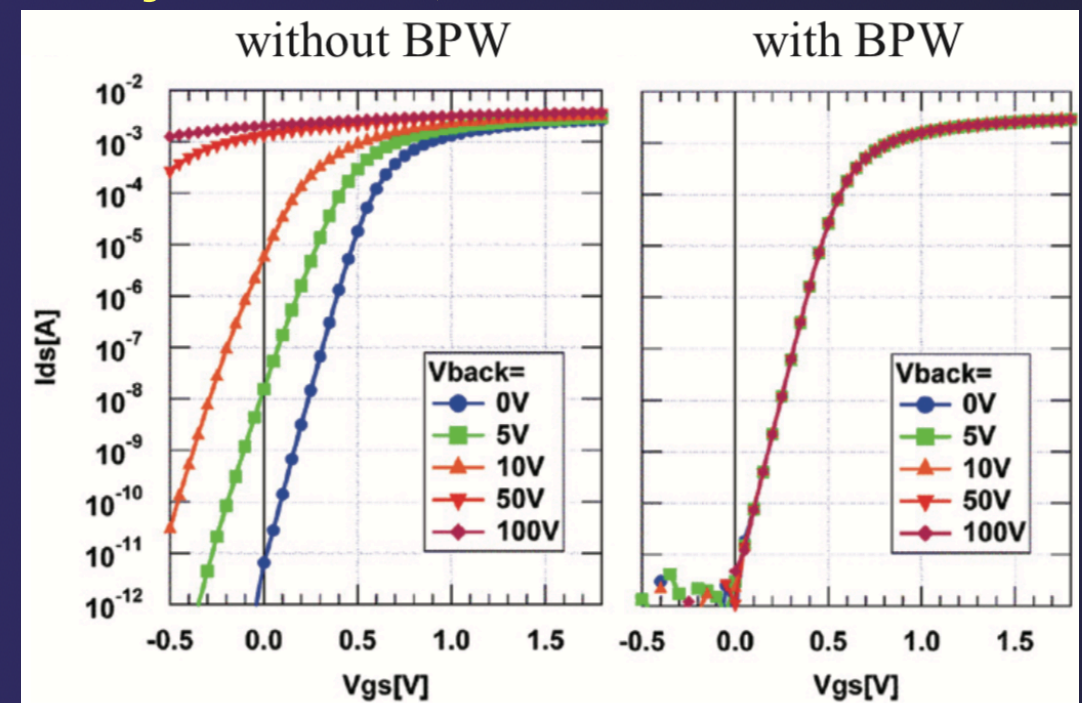
BNW used



## Back gate effect Suppression:

In SOI device, Electric field by bias voltage will affect the gate which is from PMOS or NMOS. Then the gate will affect pixel circuit operating. Using BNW structure can cover electric field then make electric field don't go into pixel circuit.

I/V curves show the difference of BPW didn't used and used. (BPW is for N wafer, SOFIST is made by P wafer )





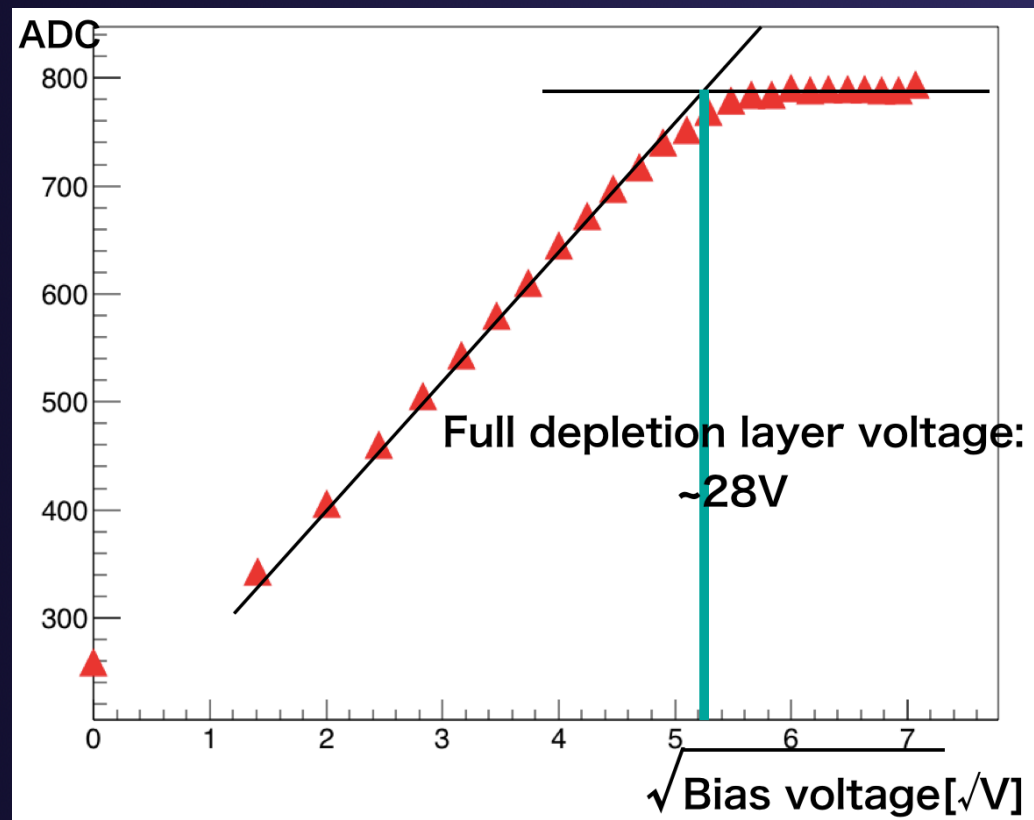
# Laser position scan

Motivation : study how depletion length and BNW affect share share & loss



Measurement parameter :

- Depletion length 3V, 13V, 30V
- BNW  $16\mu\text{m}^2, 14\mu\text{m}^2, 12\mu\text{m}^2$

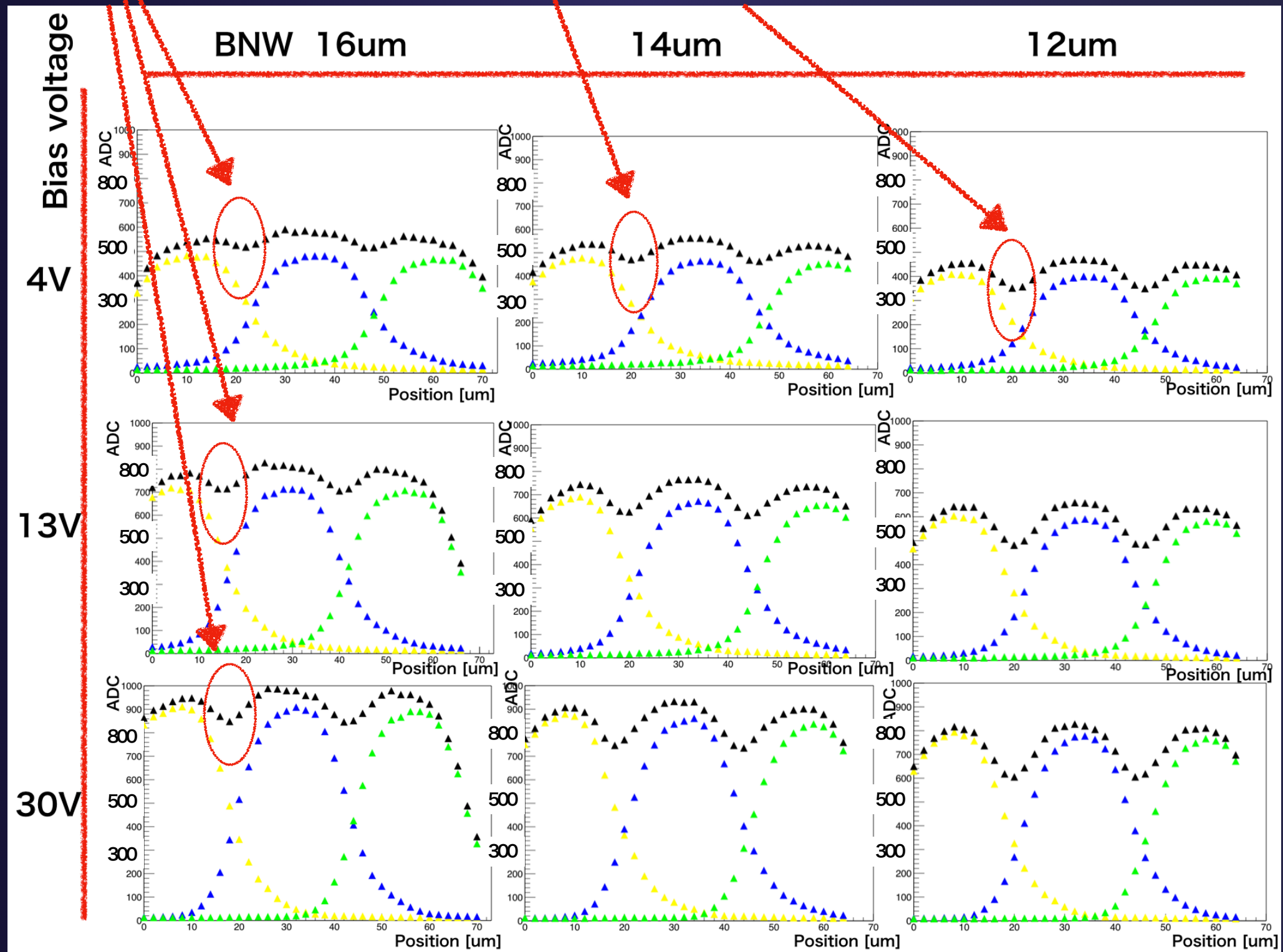




# Laser position scan

These graph shows the result of the laser scan measurement in different BNW sizes and Bias voltage.

Those “falling” show charge loss. But how can we get the information of charge loss?



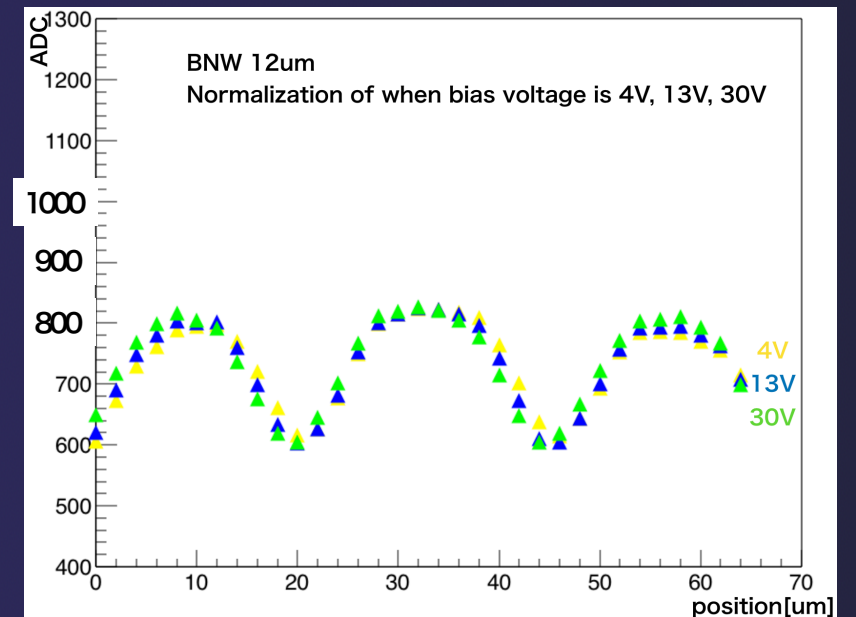
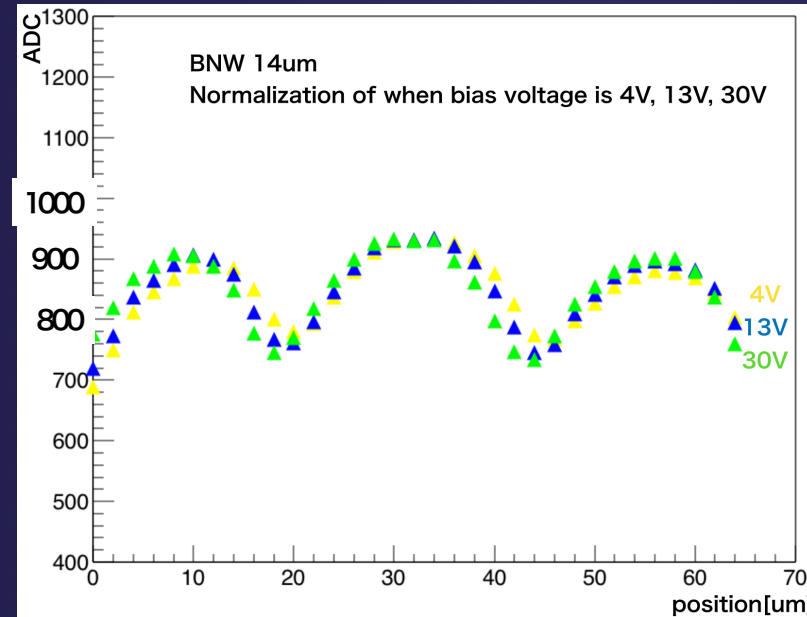
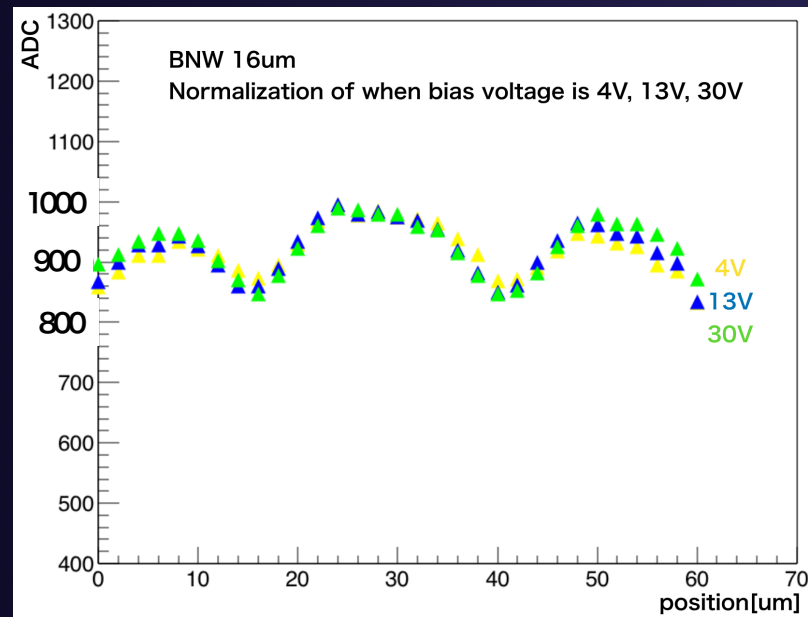


# Laser position scan

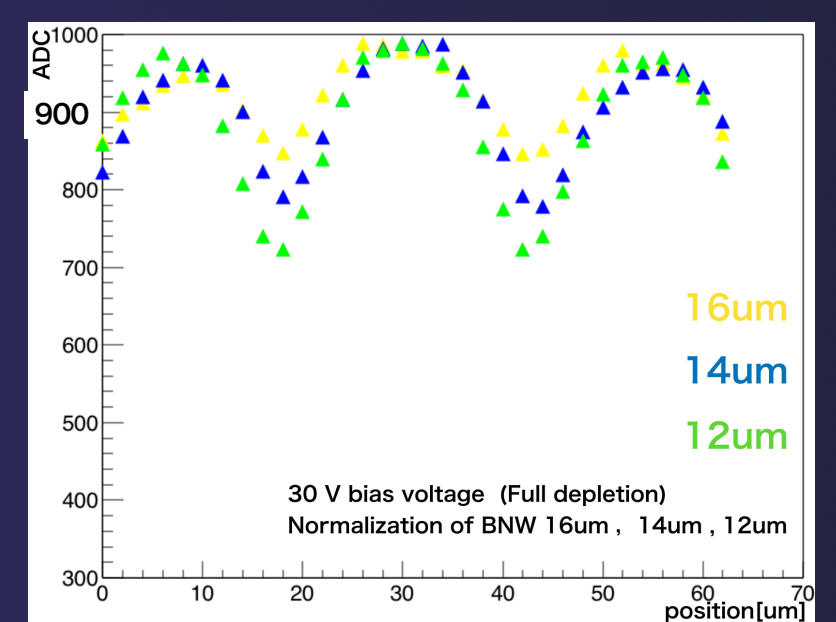
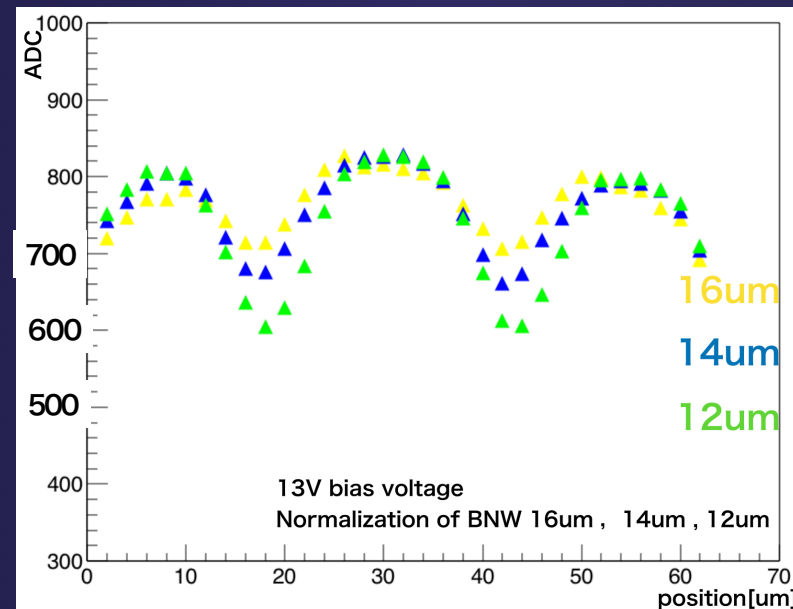
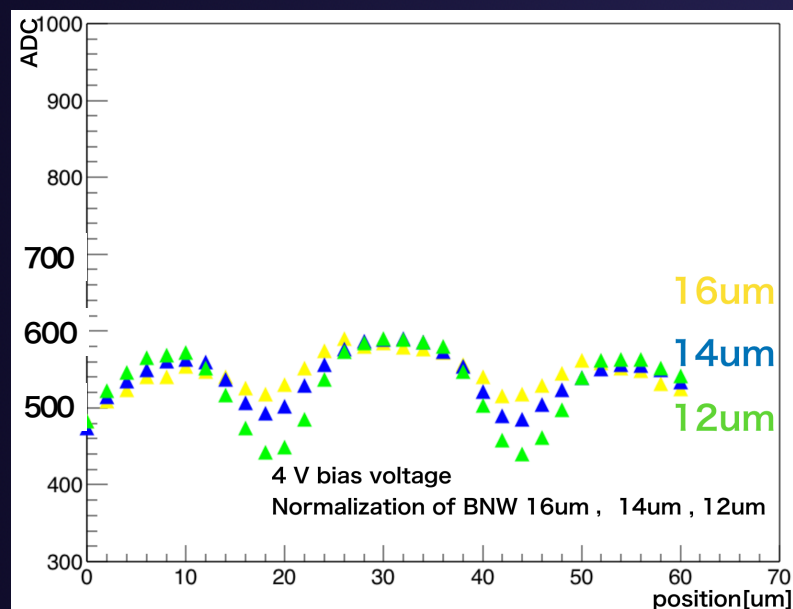
Normalized

Charge loss edge dependence

Conclusion : Charge loss is independent of depletion length



Conclusion : Charge loss is dependent of BNW size

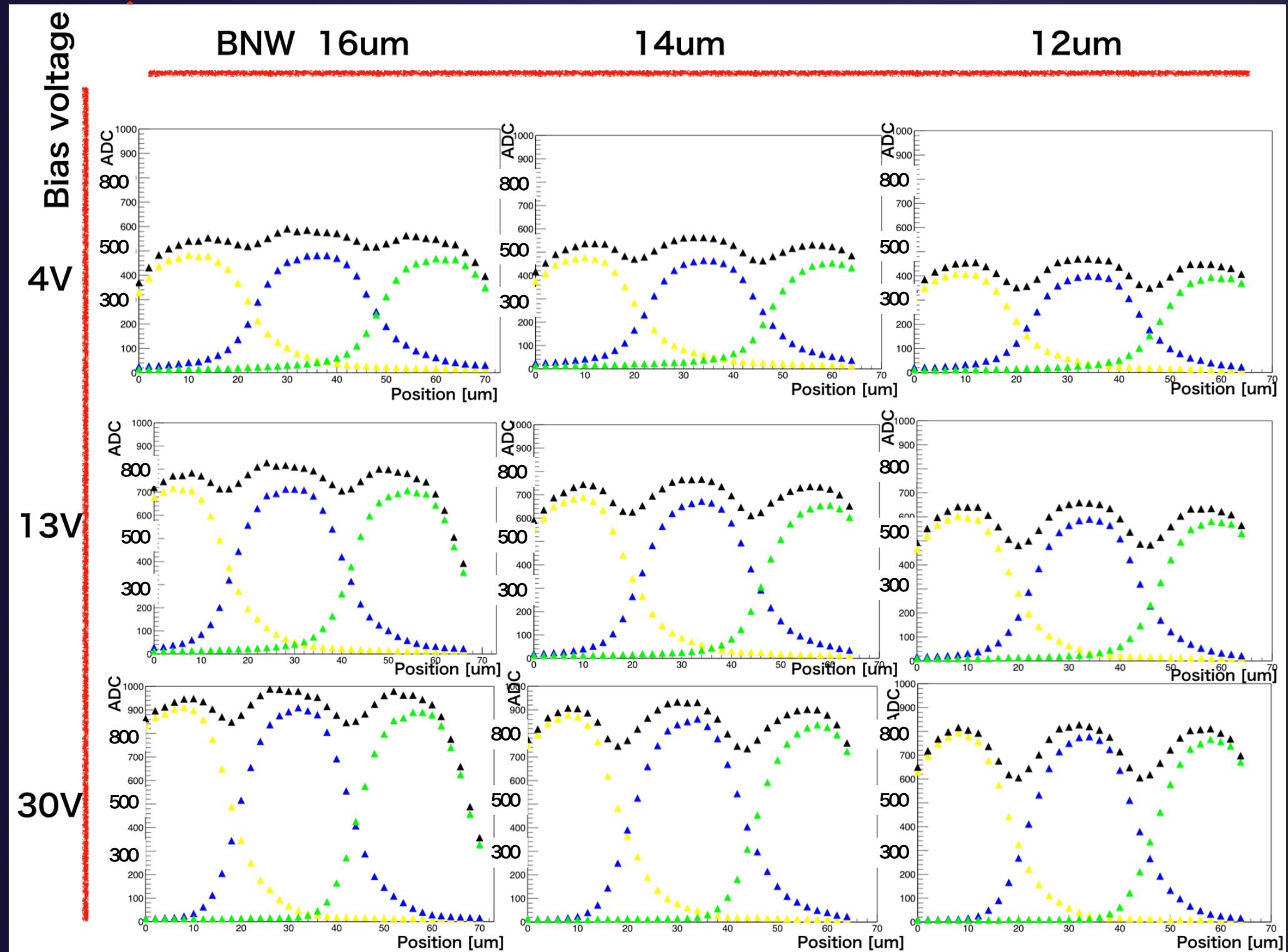




# Laser position scan

These graph shows the result of the laser position scan in different BNW sizes and Bias voltage.

This blue curve shows charge share?





# Laser position scan

error function fitting

Charge share in different BNW and depletion length

Conclusion : charge share is independent of depletion length

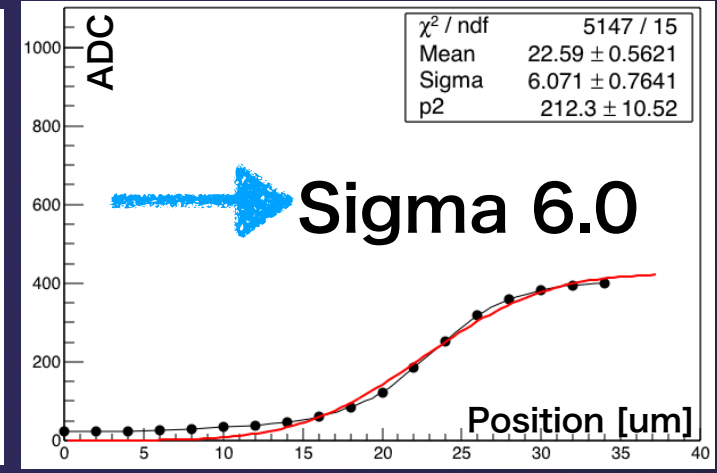
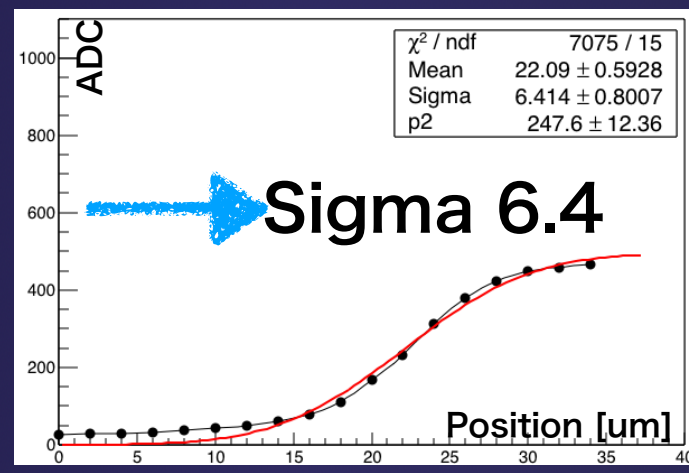
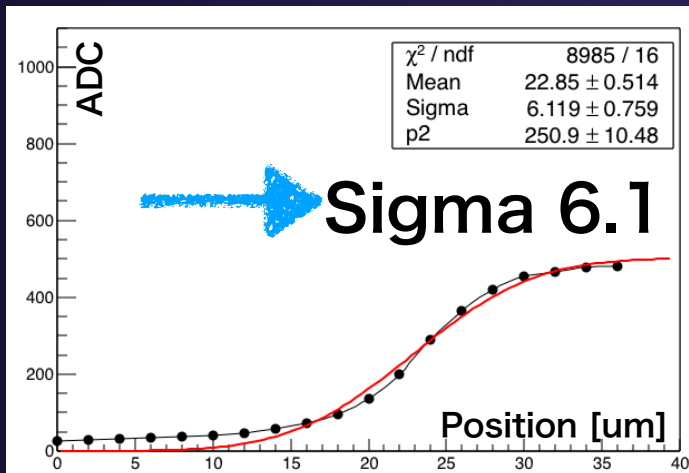
Bias voltage  
4V

BNW

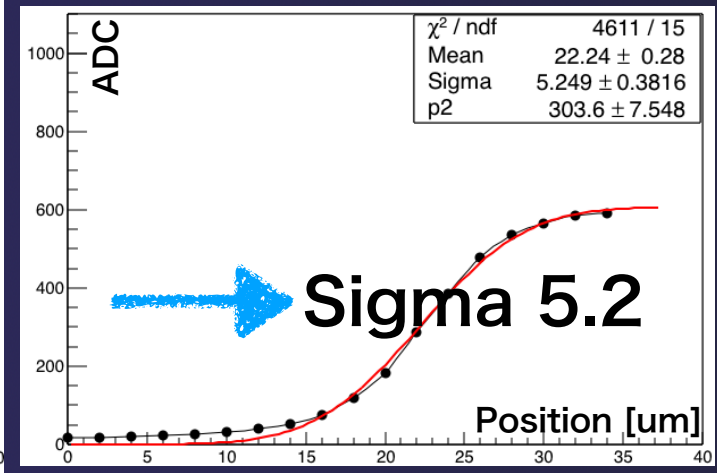
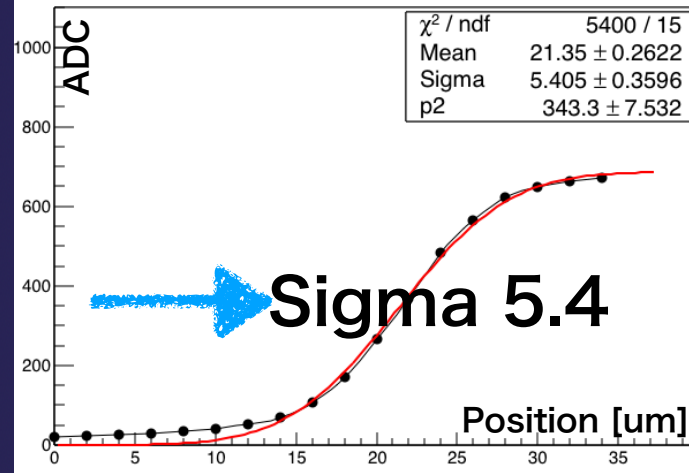
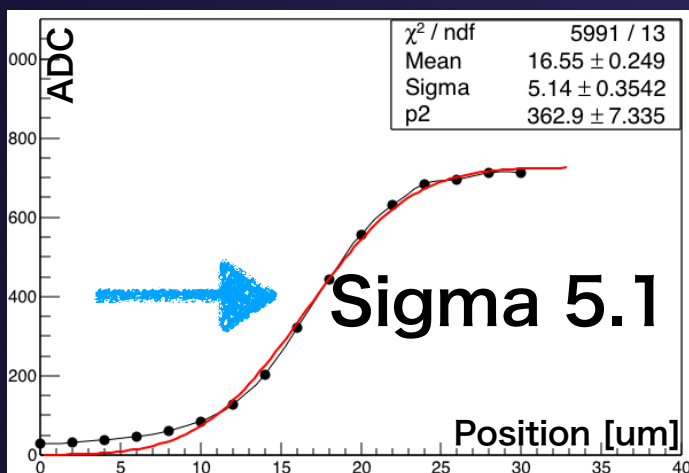
16um

14um

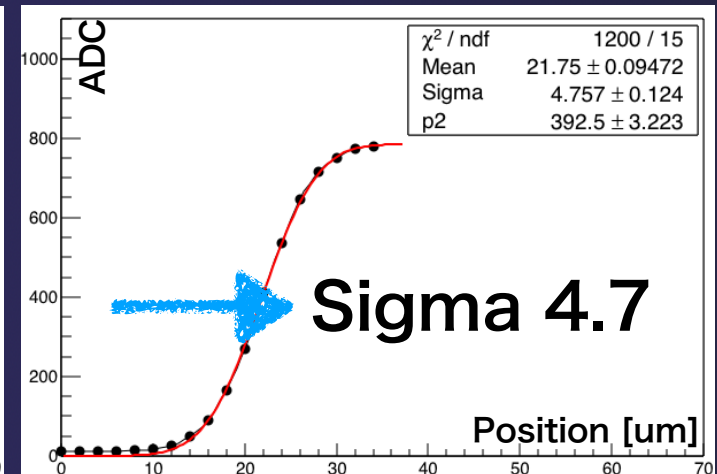
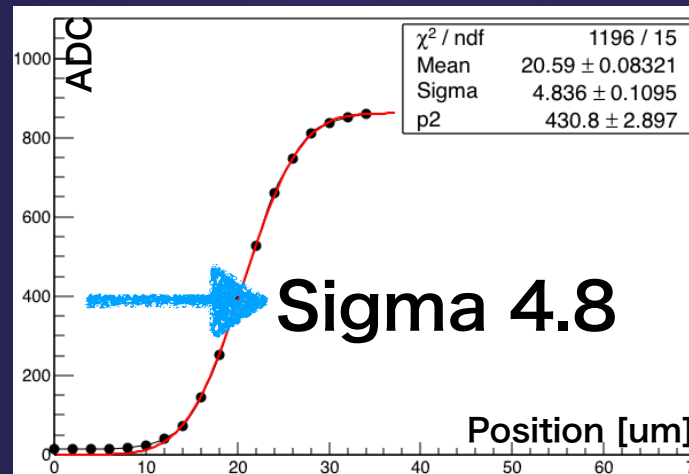
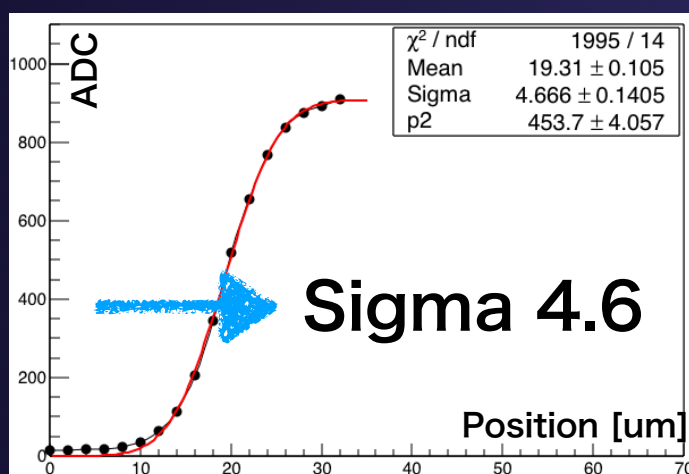
12um



13V



30V





# Summary

**SOFIST ver.2 is a pixel sensor for ILC.**

**It has a fine time resolution (730 ns) and position resolution.**

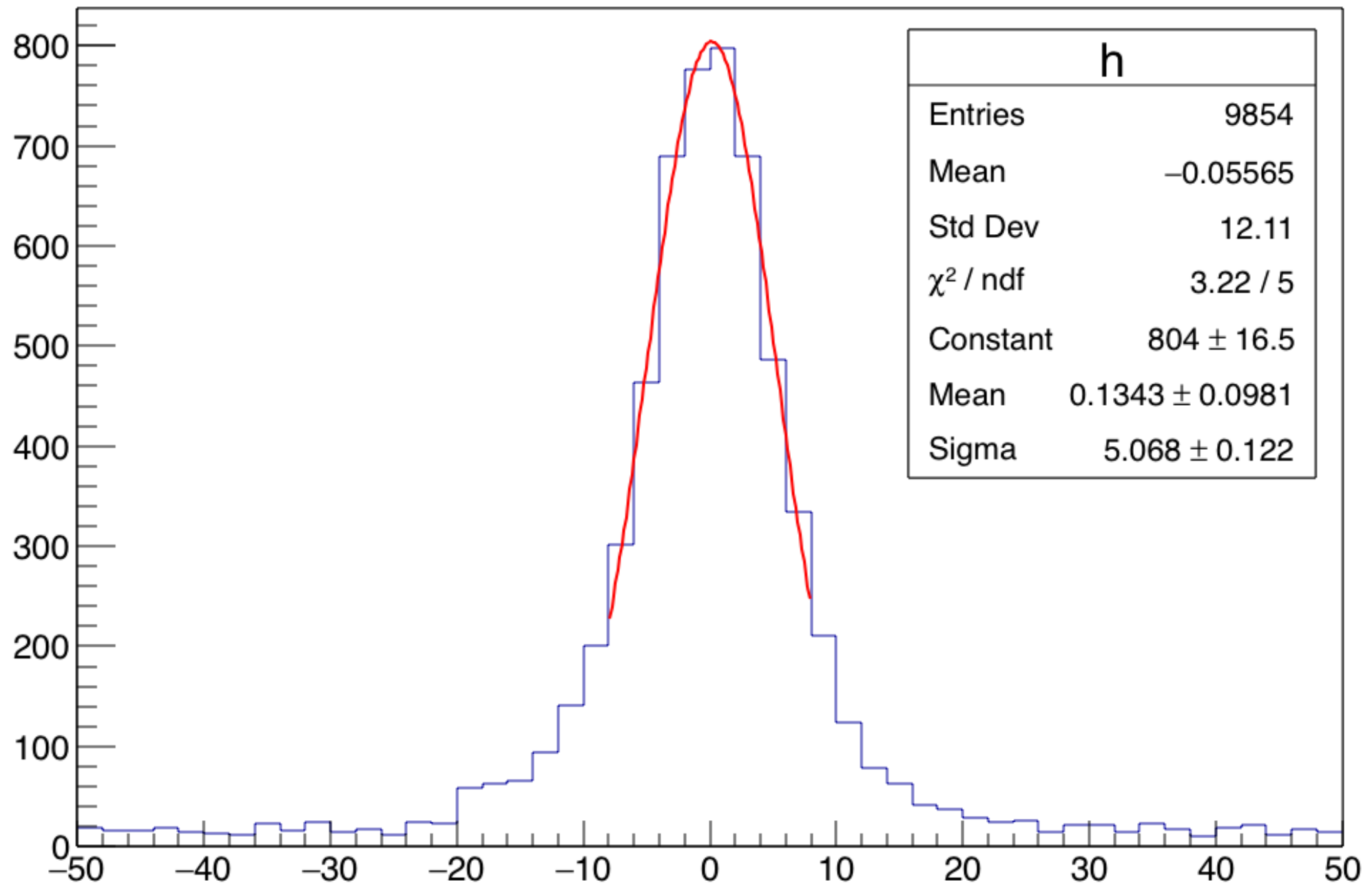
**I evaluated SOI structure and time measurement of SOFIST ver.2**



**Back up**



# time\_resolution



**Time resolution 3.58 us**



