FPGAを用いた high-resolution TDCの開発

Development of high-resolution TDC based on FPGA.

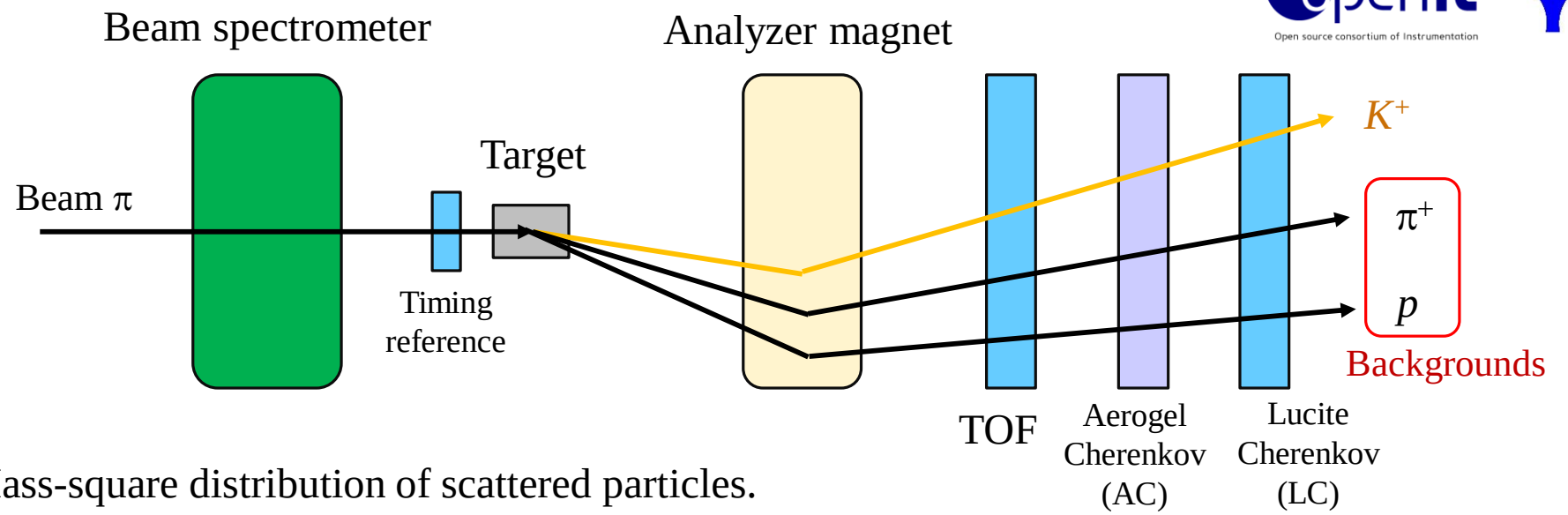
阪大理, 東北大理[A], JAEA[B], KEK[C], Open-It[D]

@本多良太郎, 三輪浩司[A], 細見健二[B],
池野正弘[CD], 内田智久[CD]

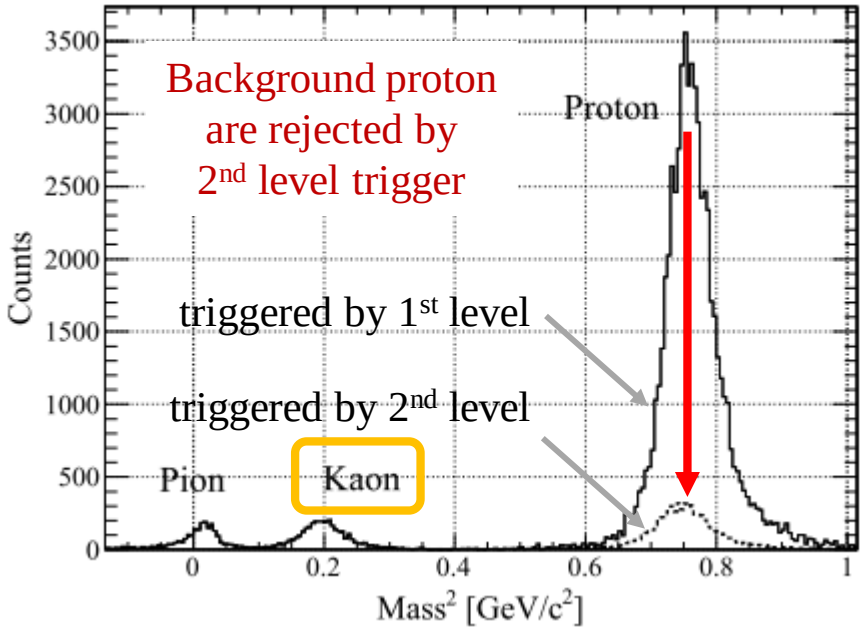
Outline

- Motivation
- Developed items
  - Hardware
  - Tapped delay line in FPGA
  - Calibration
- Performance evaluation
- Summary

Motivation



Mass-square distribution of scattered particles.

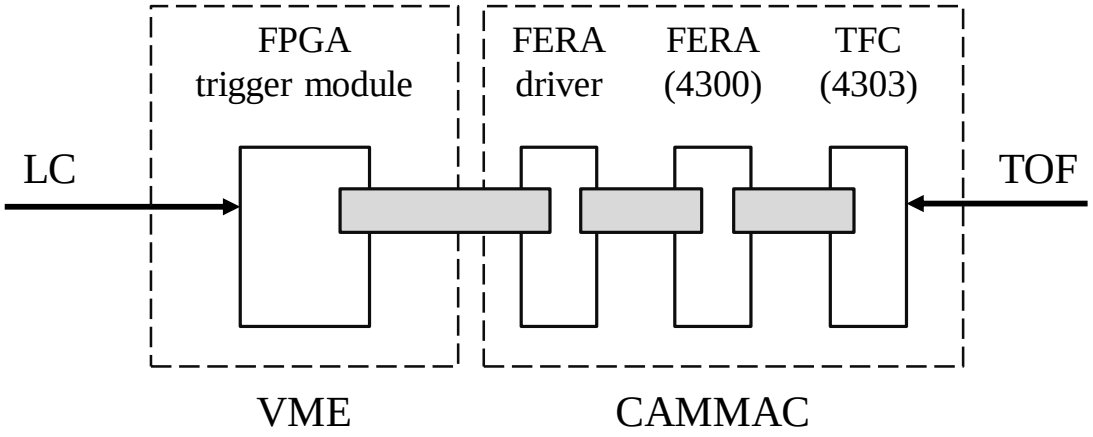


- **1st level trigger** : Coincidence of detector signals
  - Cherenkov detectors play important role.
- **2nd level trigger** : Trigger based on time-of-flight
  - High-resolution time-of-flight information is necessary.

Motivation

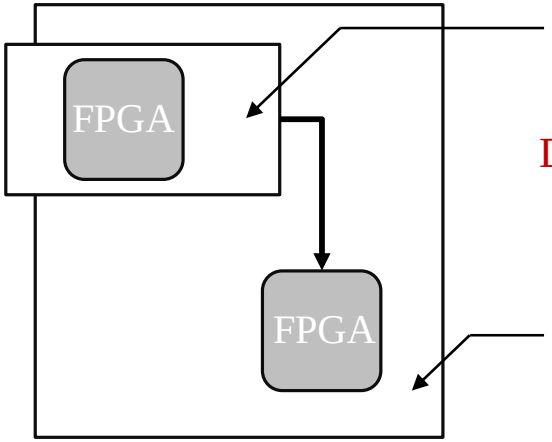
Present 2nd level trigger system

- Slow (10 μs order)
- Complex
- Old



New trigger system

- Fast (100 ns order)
- Simple



FPGA based
high-resolution TDC mezzanine card

Development of FPGA based HR-TDC is main motivation of this project.

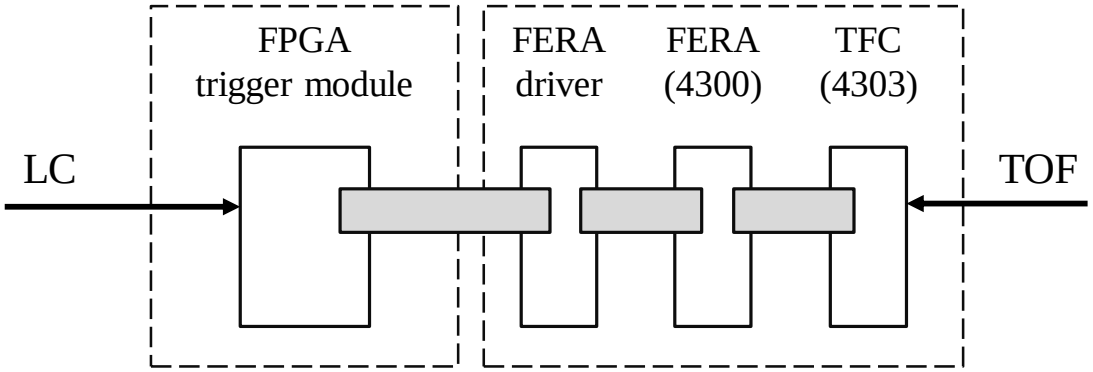
Trigger controller module
(Mother module)

Supported by Grant
新学術 (中性子星核物質) 公募研究
「J-PARC二次ビーム高強度化のための汎用トリガーモジュールの開発」

Motivation

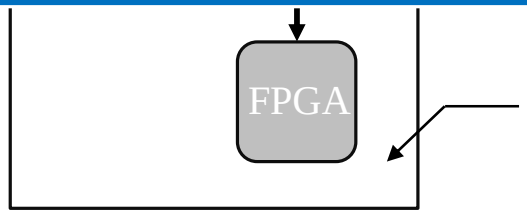
Present 2nd level trigger system

- Slow (10 μs order)
- Complex
- Old



In general, the common issue in our research field is that
no GOOD common-stop type high-resolution TDC exists.

We must overcome this problem for future experiments.

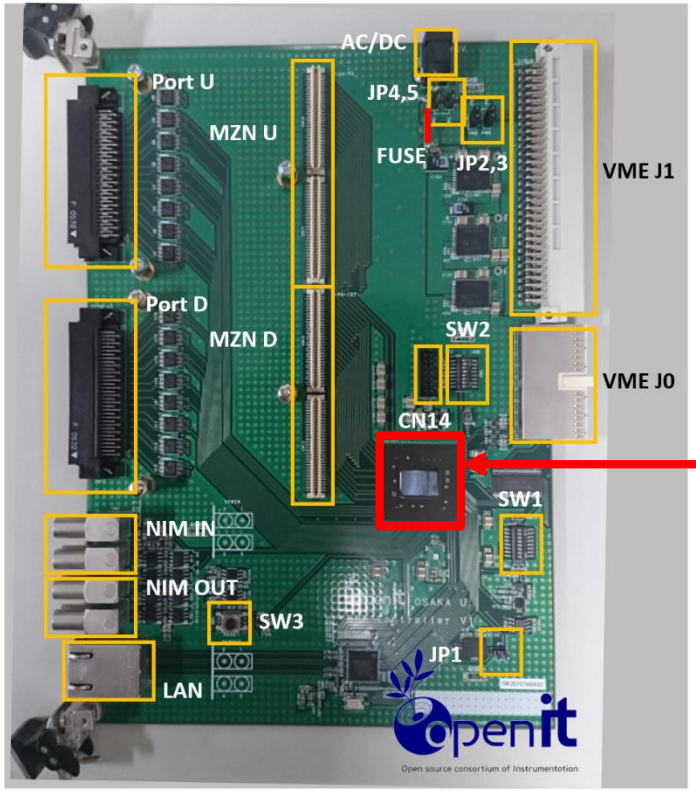


Supported by Grant
新学術 (中性子星核物質) 公募研究
「J-PARC二次ビーム高強度化のための汎用トリガーモジュールの開発」

Developed hardware

Hadron universal logic (HUL) controller module

HUL mezzanine cards



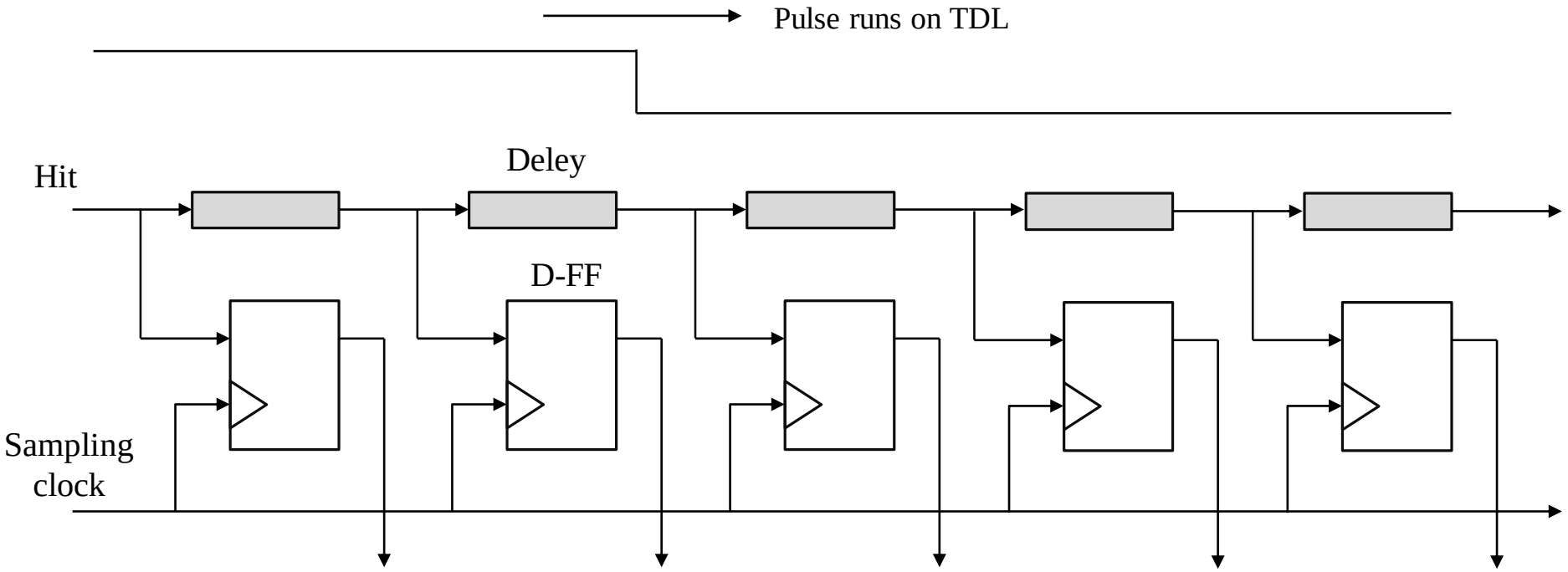
Today's topic is implementation of HR-TDC into Xilinx Kintex7 160T on HUL controller.

- 64ch ECL/LVDS inputs
- Two mezzanine slots
- GbE : SiTCP (VME communication is not supported)
- Powered by J1 or AC adaptor (5V)

This project is technically supported by Open-It.
http://openit.kek.jp/project/HUL/public/hul

Principle of Tapped Delay Line HR-TDC

Tapped Delay Line (TDL)



D-Flip-Flop captures the snapshot of the pulse running on TDL.

Implementation of TDL into FPGA

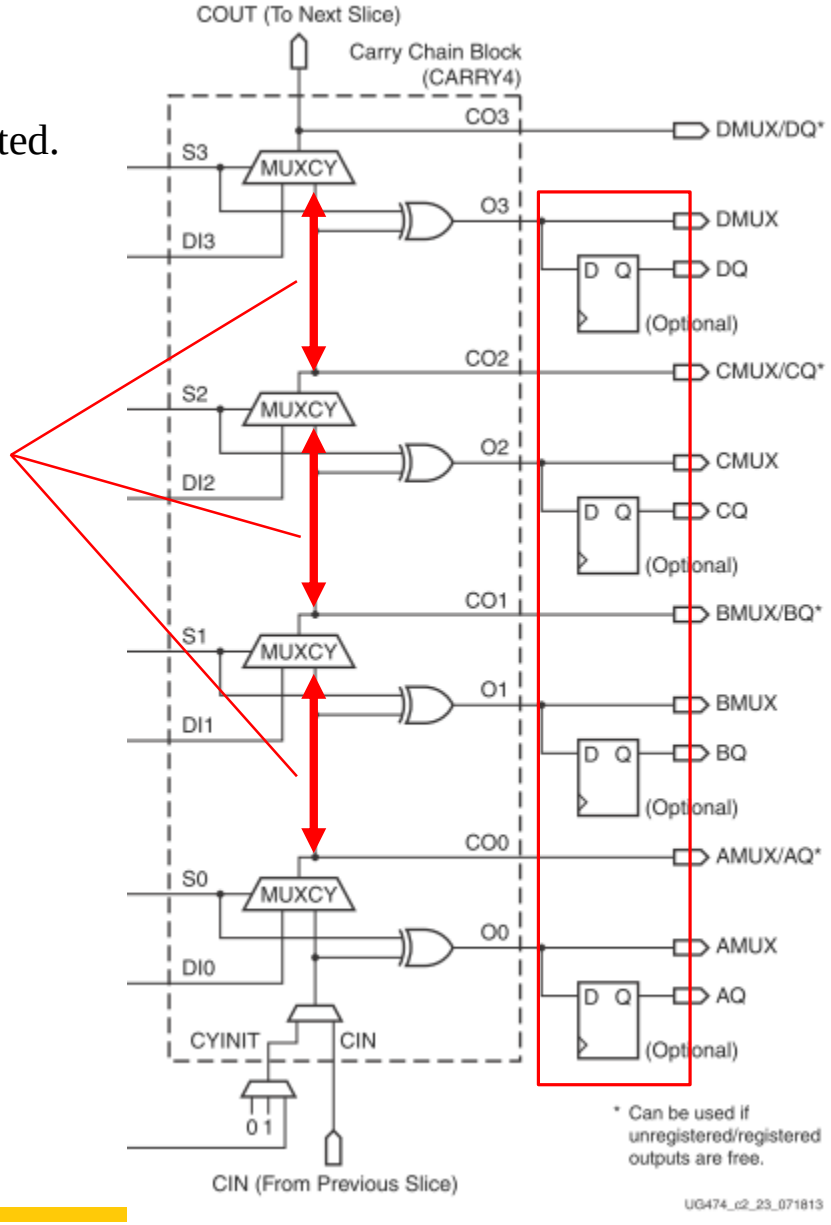
FPGA : Field-Programmable Gate Array

- Gate level logic coded by users can be implemented.

Implement TDL using carry line in FPGA

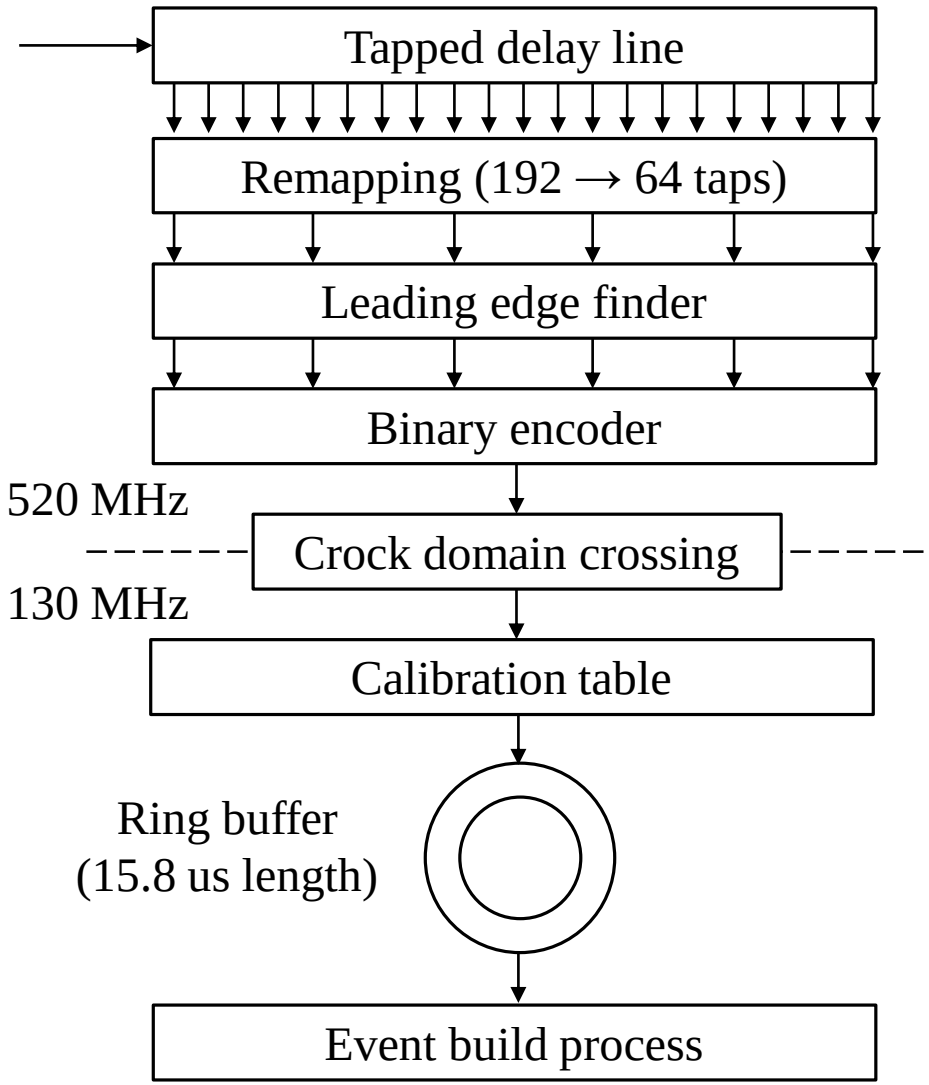
Carry line

- Basic function of Adder
- Smallest delay element with 5-30 ps delay time
- Close to FF
- Cascadable



Xilinx UG474

Implemented logic



Pulse run →

1111111111111000000000000000

1111100000

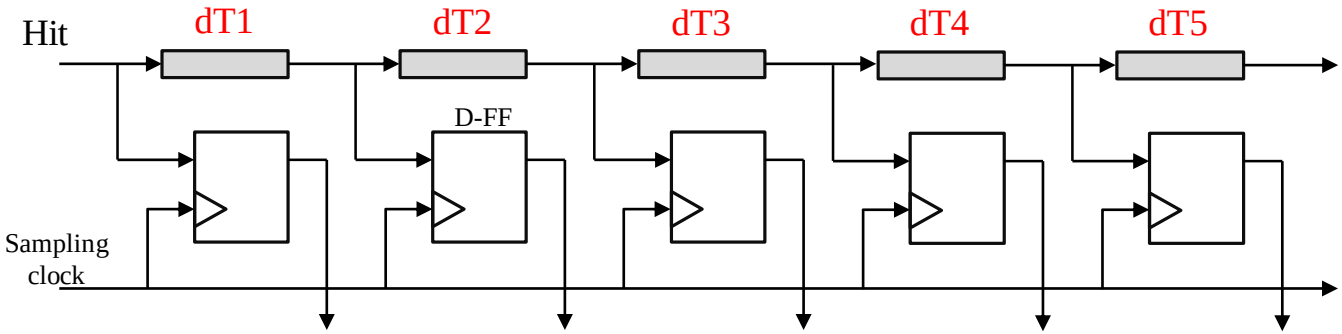
0000100000

5 : Fine count
+
Semi coarse count (2bit)
+
Coarse count (11bit)

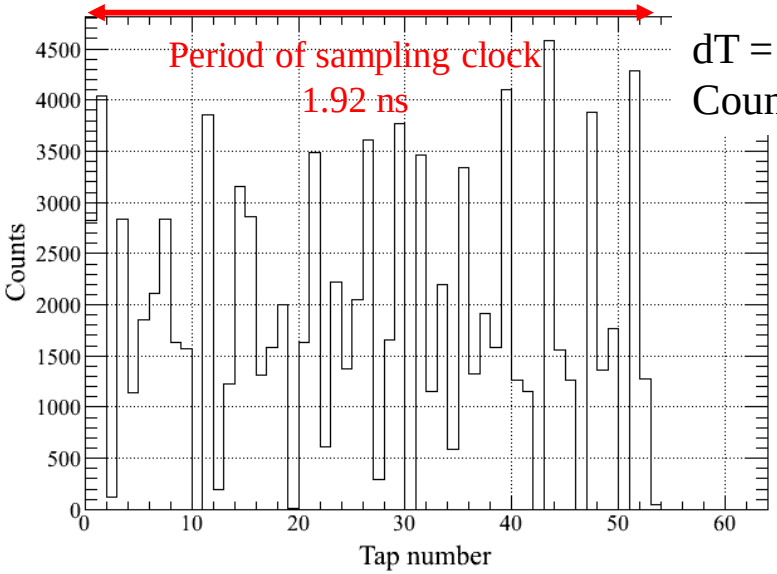
32ch HR-Timing unit and DAQ functions were fully implemented into Kintex7 160T.

Distribution of delay time

Delay time (dT) is not constant.

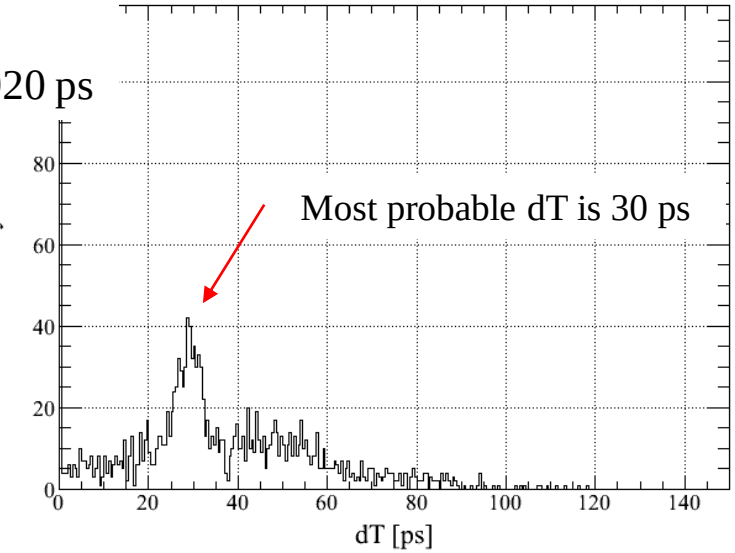


Tap number histogram

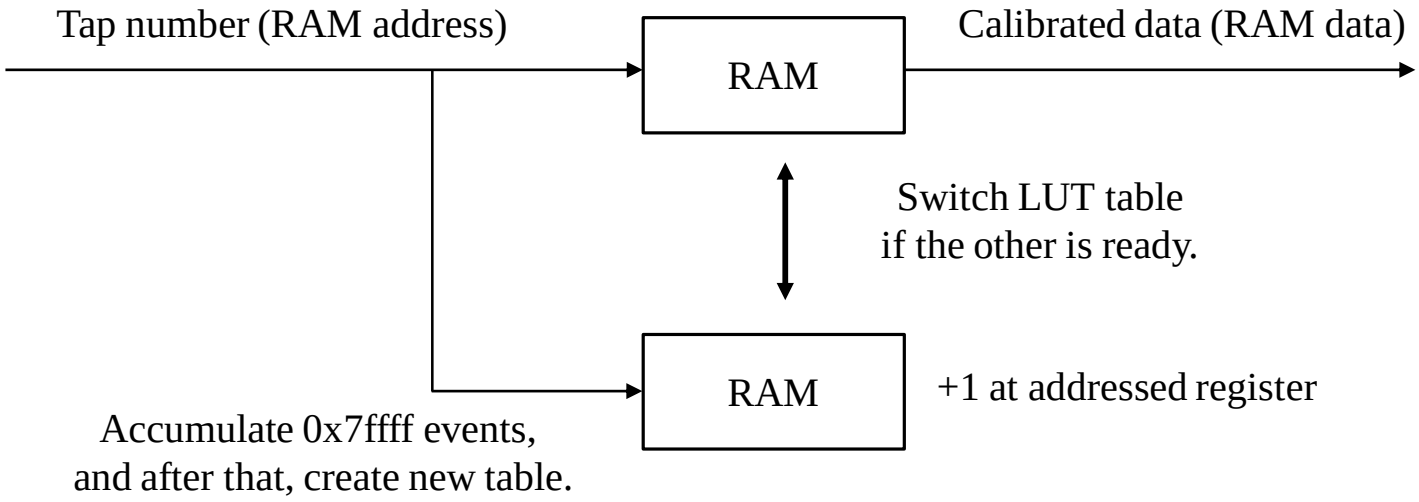


dT = Count/TotalEntry*1920 ps

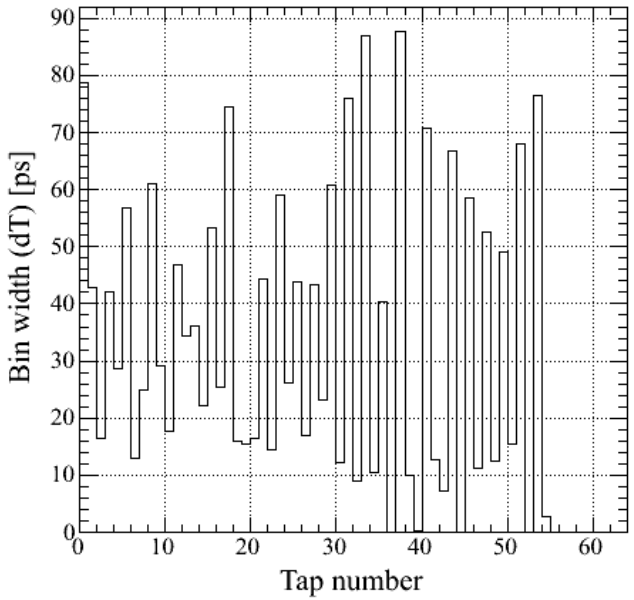
dT distribution for all the channels



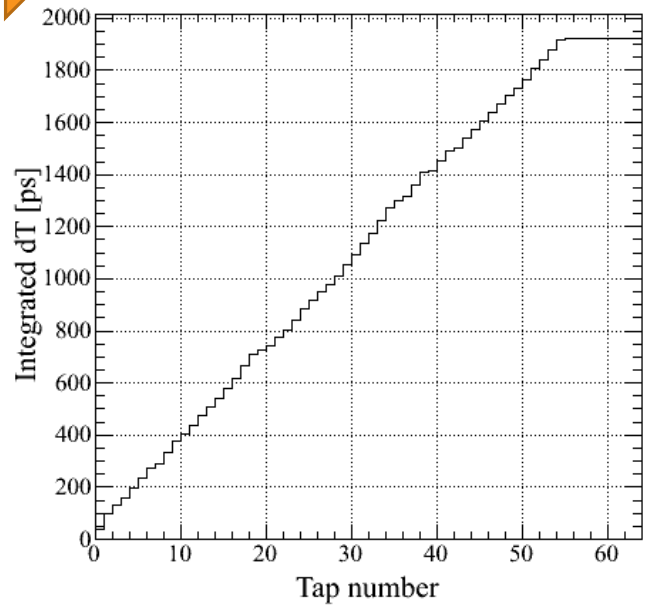
Calibration of TDL



Tap number histogram



Calibrated look up table



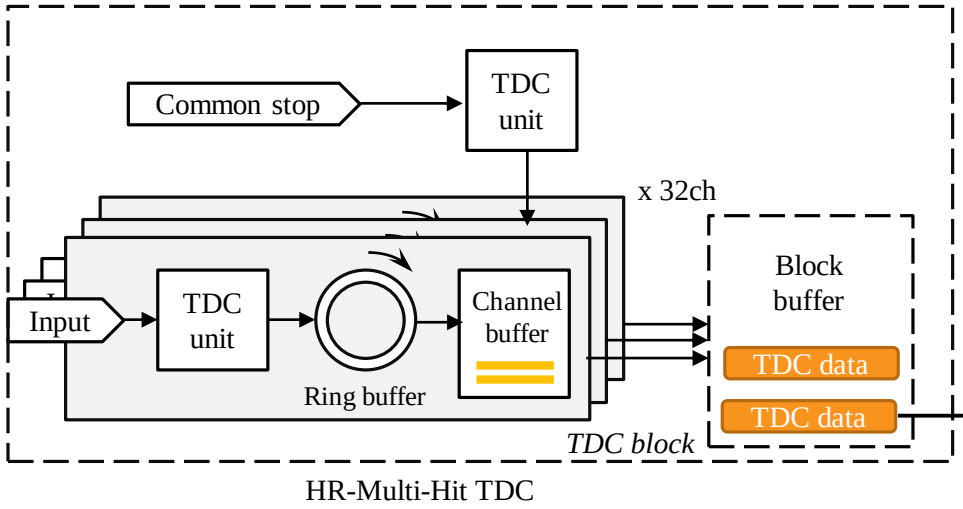
Nth Val =
$w_n/2 + \Sigma^{n-1}_0 (w_i)$

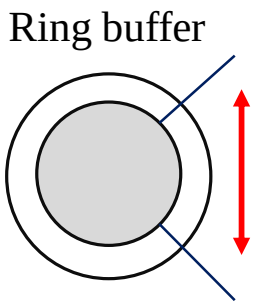
Calibration of method

- Use detector signal.
  - Corresponding to that the clock sampling of the detector signal. The detector signal must be random.

- Use clock.
  - The TDC clock is 520 MHz (f_{sample}) and calibration clock is 26.2144 (f_{calib})
  - $N*(f_{sample}/f_{calib}) = N*(2^{9}*5^{7}*13)/(2^{20}*5^{2}) = N*(5^{5}*13)/\mathbf{2^{11}}$
  - 2048 different clock phases appear

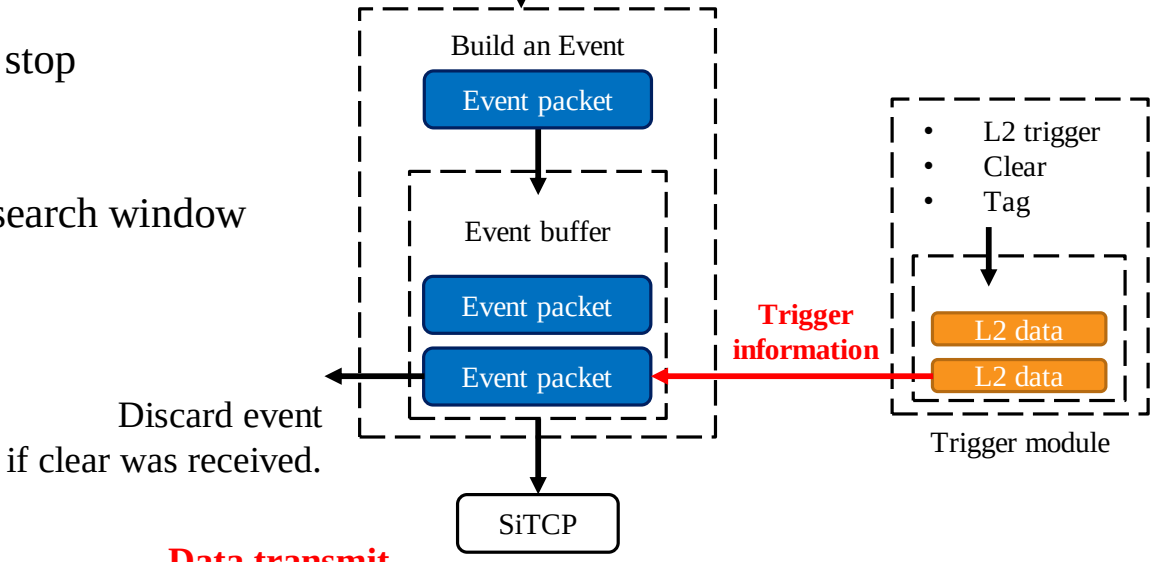
DAQ functions





Hits inside the search window are stored in channel buffer, when trigger is received.

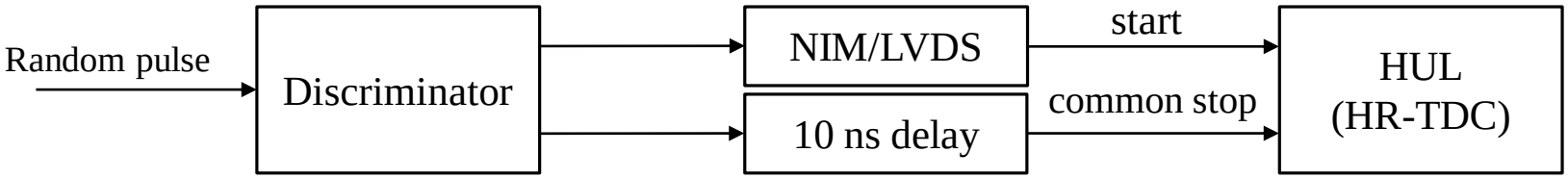
Channel : 32
Trigger type : Common stop
Ring buffer length : 15.8 us
MaxHit/ch/event : 16
Dead time : Equal to search window



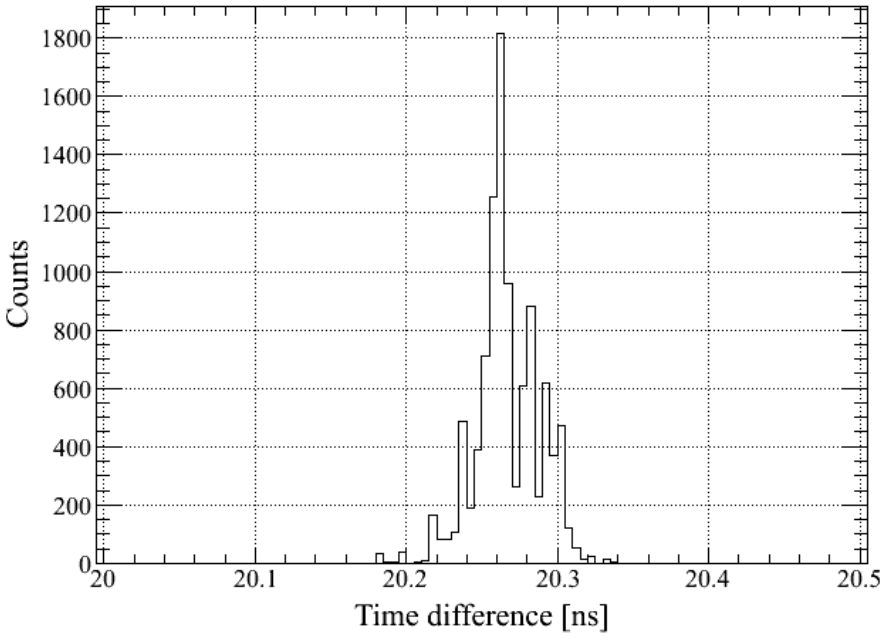
Data transmit if L2 was received.

Performance evaluation

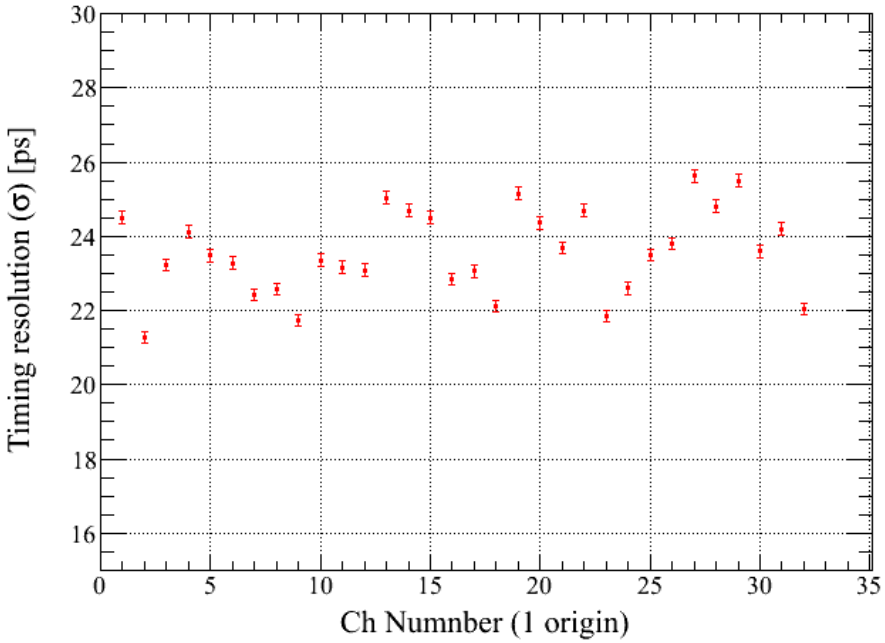
Timing resolution



Timing distribution
between ch1 and common stop



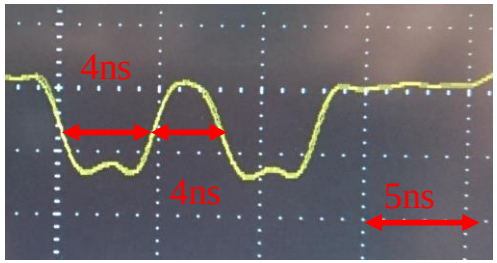
Timing resolution
between each channel and common stop



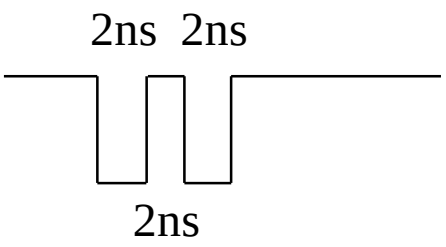
Timing resolution better than 30 ps (σ) achieved for all the channel !

Double hit resolution

Input pulse

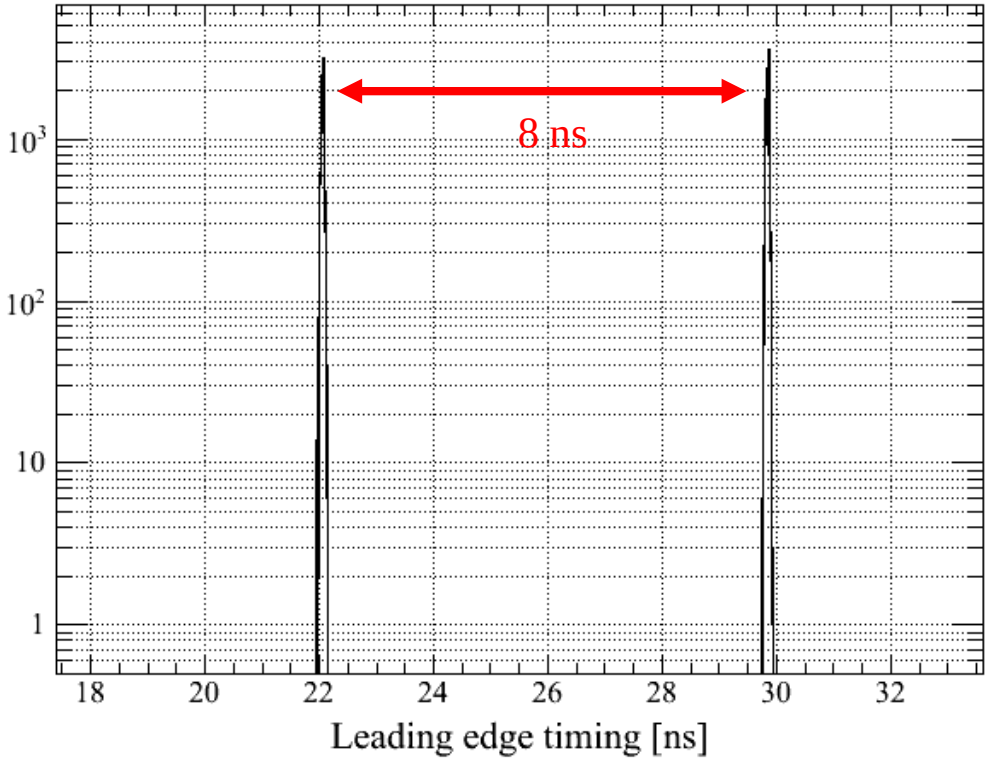


Double pulse could be measured with 100% efficiency.



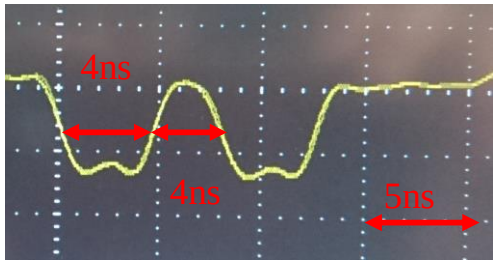
In principle, double pulses with quite short interval can be measured .

Measured timing distribution

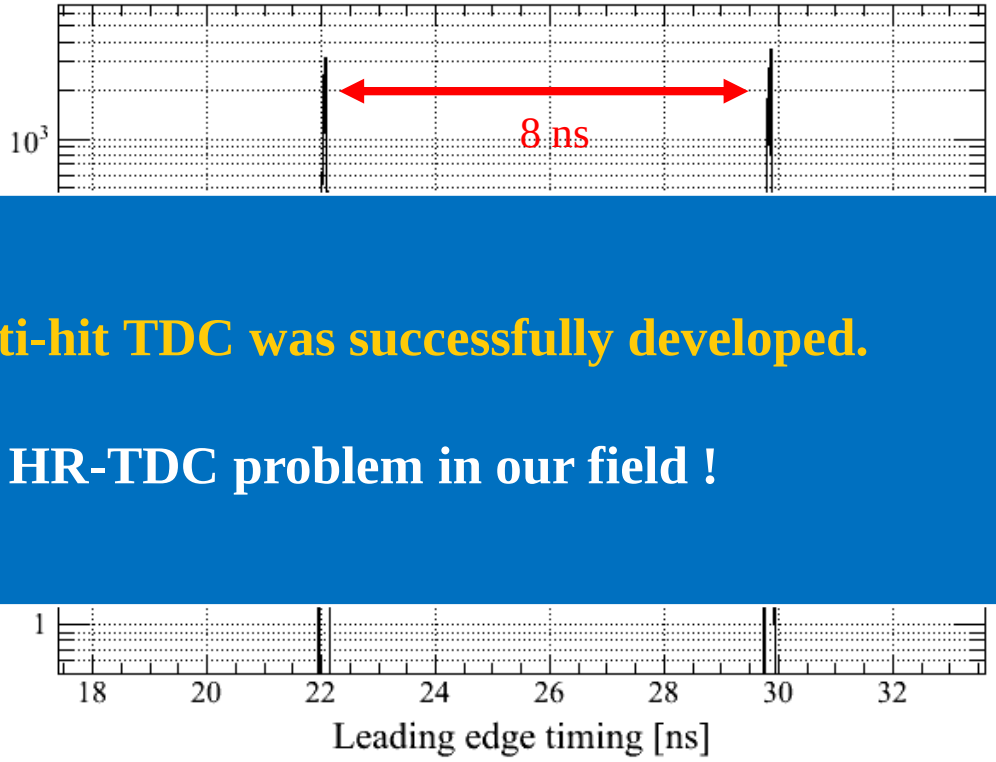


Double hit resolution

Input pulse



Measured timing distribution



High-resolution multi-hit TDC was successfully developed.

We overcame HR-TDC problem in our field !

2ns

In principle, double pulses with quite short interval can be measured .

ToDo

Implement both leading and trailing edges measurement.

- At present, 8ch leading/trailing measurement was achieved.

Implement HR-TDC to FPGA on mezzanine card.

- Separate HR-TDC part from the DAQ functions.
- Customization of DAQ functions can be easy.

Future possibility

- Synchronization with master clock
- Implement as free-run type TDC

New mezzanine card for HR-TDC
(Same FPGA is mounted)

Summary

- Develop the 2nd level trigger system using FPGA based HR-TDC for the K^+ selection in J-PARC experiments.
- Furthermore, FPGA based HR-TDC solve the problem that no good HR-TDC exists in our research field.

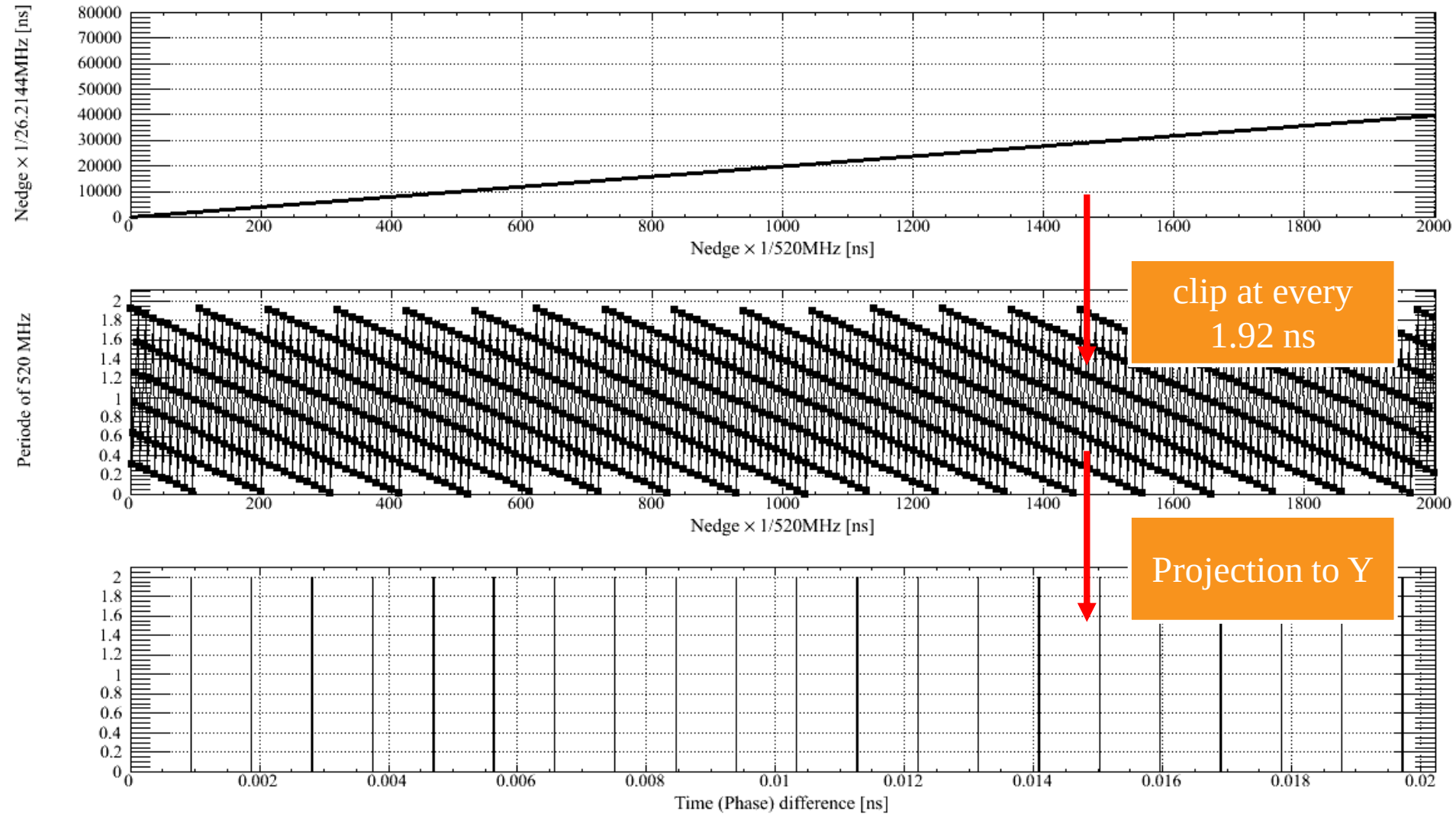
- Tapped delay line HR-TDC, which realized by carry line, was implemented into Xilinx Kintex7 160T.
- **32ch HR-TDC unit and DAQ functions were fully implemented.**

- **The timing resolution better than 30 ps (σ)** was achieved for all the channel.
- The double-hit resolution was at least 8 ns.

- **We overcame the HR-TDC problem by this development.**

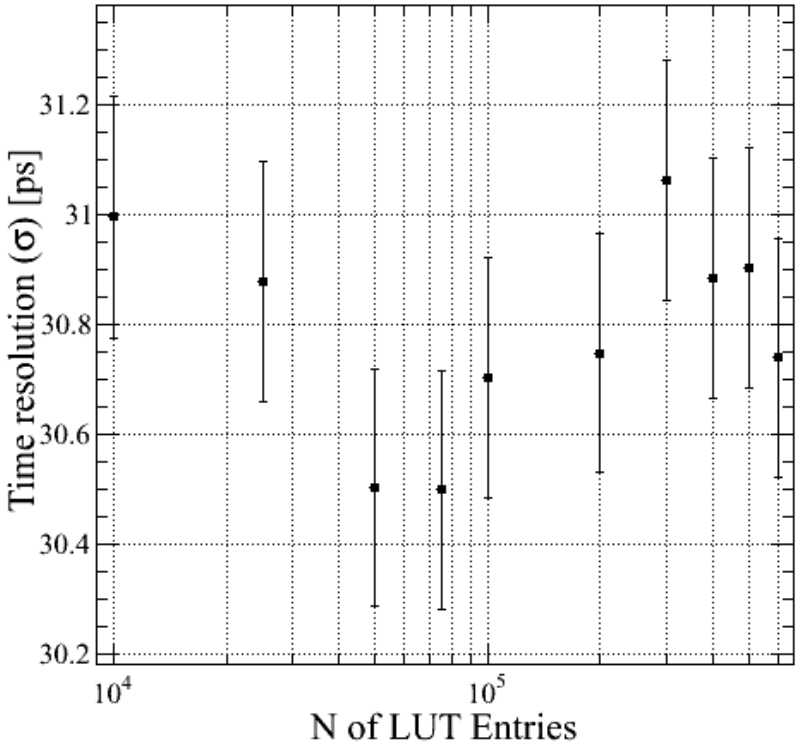
Backup

Principle of calibration using clock.

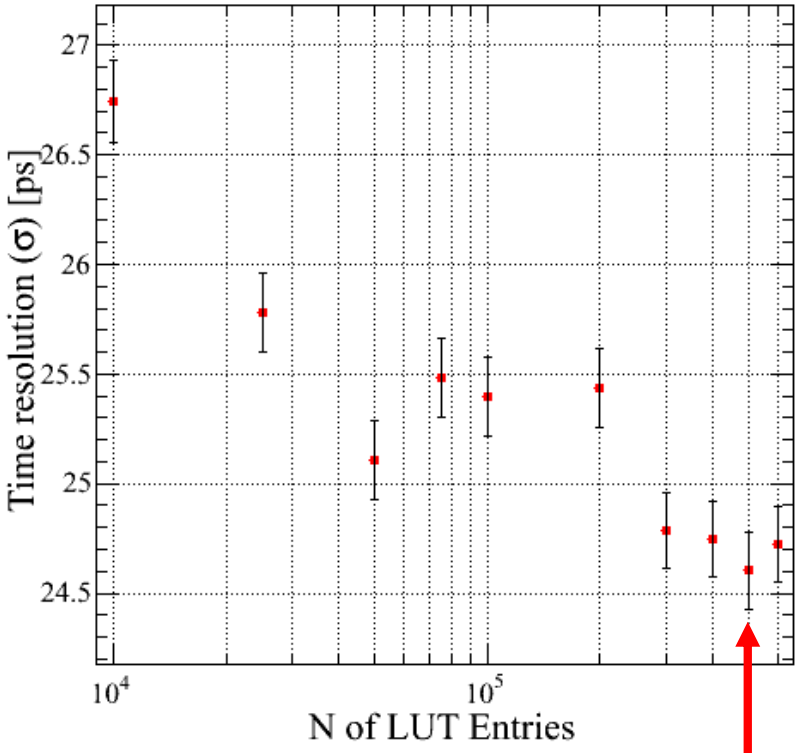


LUT Entry dependence of timing resolution

Timing resolution of ch0-ch1 (NIM)



Timing resolution of ch2-ch3 (ECL)

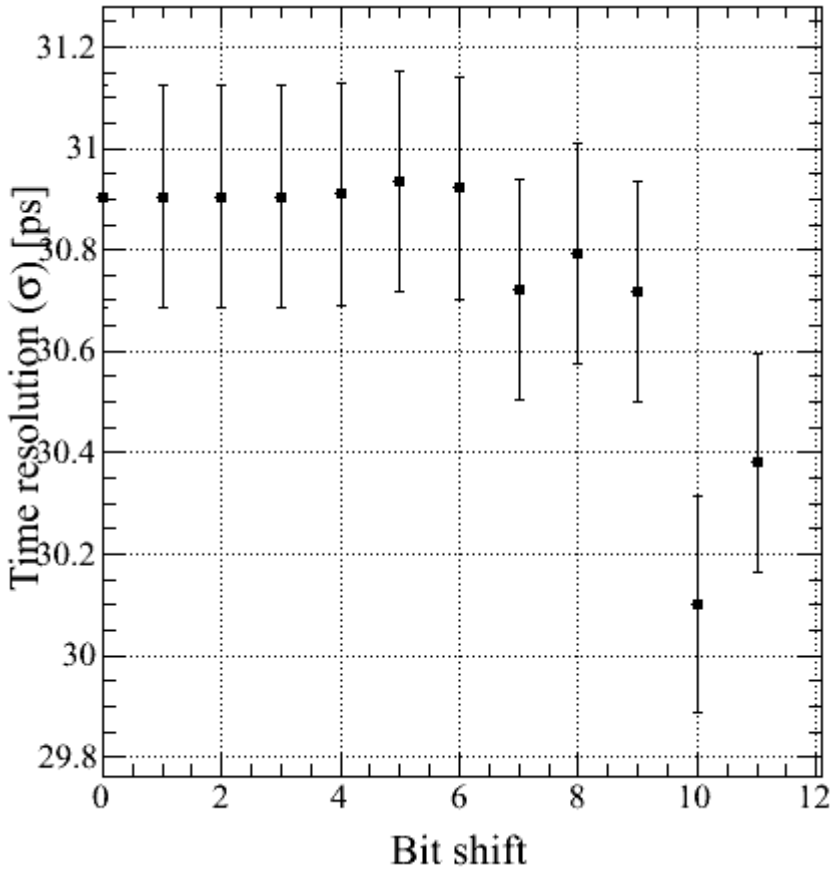


Present setting

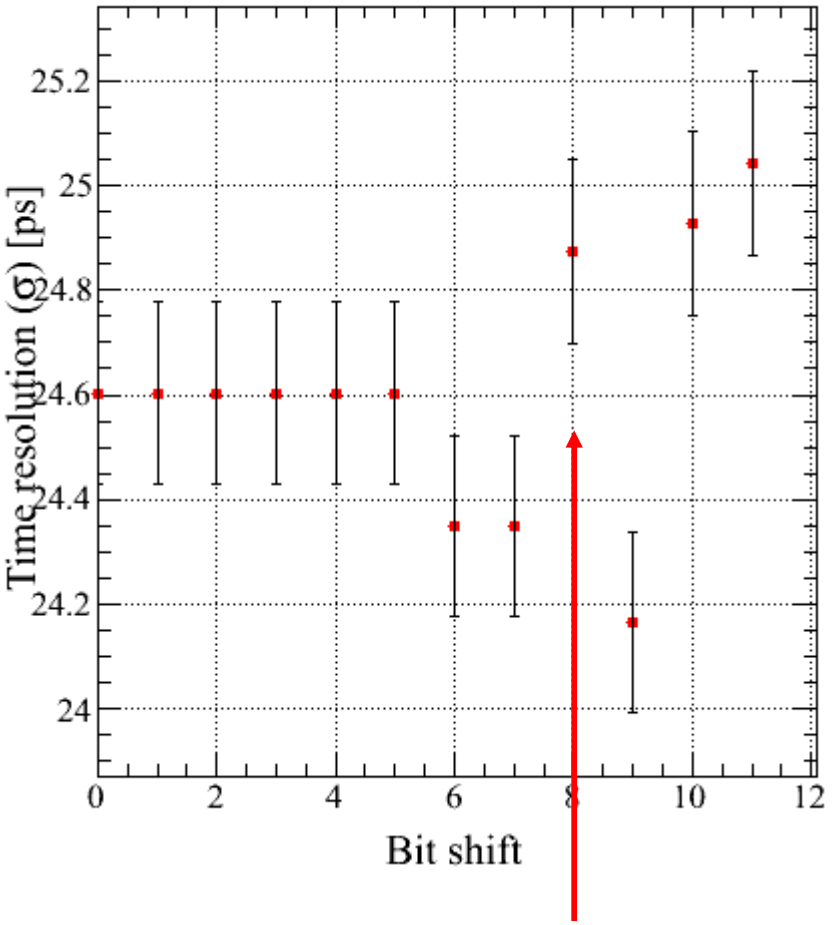
At present, LUT table accumulate 0x7ffff events.

Bit length dependence of timing resolution

Timing resolution of ch0-ch1 (NIM)



Timing resolution of ch2-ch3 (ECL)



At present, lower 8bits are discarded.