Development of high-resolution TDC based on FPGA.

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Outline

• Motivation
• Developed items
  • Hardware
  • Tapped delay line in FPGA
  • Calibration
• Performance evaluation
• Summary
Motivation

Beam spectrometer

Analyzer magnet

Beam π
Target
Timing reference

TOF
Aerogel Cherenkov (AC)
Lucite Cherenkov (LC)

Backgrounds

Mass-square distribution of scattered particles.

- **1st level trigger**: Coincidence of detector signals
  - Cherenkov detectors play important role.

- **2nd level trigger**: Trigger based on time-of-flight
  - High-resolution time-of-flight information is necessary.

Background proton are rejected by 2nd level trigger

triggered by 1st level

triggered by 2nd level

Proton
Pion
Kaon
Motivation

Present 2nd level trigger system

- Slow (10 μs order)
- Complex
- Old

New trigger system

- Fast (100 ns order)
- Simple

Supported by Grant
新学術 (中性子星核物質) 公募研究「J-PARC二次ビーム高強度化のための汎用トリガーモジュールの開発」
Motivation

**Present 2nd level trigger system**

- Slow (10 μs order)
- Complex
- Old

In general, the common issue in our research field is that no GOOD common-stop type high-resolution TDC exists.

We must overcome this problem for future experiments.

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Developed hardware

Hadron universal logic (HUL) controller module

HUL mezzanine cards

This project is technically supported by Open-It.
http://openit.kek.jp/project/HUL/public/hul

- 64ch ECL/LVDS inputs
- Two mezzanine slots
- GbE : SiTCP (VME communication is not supported)
- Powered by J1 or AC adaptor (5V)

Today’s topic is implementation of HR-TDC into Xilinx Kintex7 160T on HUL controller.
Principle of Tapped Delay Line HR-TDC

Tapped Delay Line (TDL)

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D-Flip-Flop captures the snapshot of the pulse running on TDL.
Implementation of TDL into FPGA

FPGA: Field-Programmable Gate Array
- Gate level logic coded by users can be implemented.

Implement TDL using carry line in FPGA

Carry line
- Basic function of Adder
- Smallest delay element with 5-30 ps delay time
- Close to FF
- Cascadable

Xilinx UG474
Implemented logic

Pulse run

1111111111111100000000000000000

1111100000

0000100000

5 : Fine count
  +
  Semi coarse count (2bit)
  +
  Coarse count (11bit)

32ch HR-Timing unit and DAQ functions were fully implemented into Kintex7 160T.
Distribution of delay time

Delay time (dT) is not constant.

Tap number histogram

\[ dT = \frac{\text{Count}}{\text{TotalEntry}} \times 1920 \text{ ps} \]

Most probable \( dT \) is 30 ps
Calibration of TDL

Tap number (RAM address) → RAM → Calibrated data (RAM data)

Switch LUT table if the other is ready.

Accumulate 0x7fffff events, and after that, create new table.

Tap number histogram

Calibrated look up table

Nth Val = \( w_n/2 + \sum_{i=0}^{n-1} (w_i) \)
Calibration of method

• Use detector signal.
  • Corresponding to that the clock sampling of the detector signal. The detector signal must be random.

• Use clock.
  • The TDC clock is 520 MHz ($f_{\text{sample}}$) and calibration clock is 26.2144 ($f_{\text{calib}}$)
  • $N*(f_{\text{sample}}/f_{\text{calib}}) = N*(2^9*5^7*13)/(2^{20}*5^2) = N*(5^5*13)/2^{11}$
  • 2048 different clock phases appear
DAQ functions

- **Channel**: 32
- **Trigger type**: Common stop
- **Ring buffer length**: 15.8 us
- **MaxHit/ch/event**: 16
- **Dead time**: Equal to search window

Ring buffer

- Hits inside the search window are stored in channel buffer, when trigger is received.

**Data transmit**

if L2 was received.

- **Discard event**
  - if clear was received.

- **Build an Event**
  - **Event packet**
    - Event buffer
      - **Event packet**
        - **Event packet**
          - **SiTCP**

- **Trigger module**
  - **L2 trigger**
  - **Clear**
  - **Tag**

**HR-Multi-Hit TDC**

- **Input**
  - **TDC unit**
    - **Ring buffer**
      - **x 32ch**
        - **Channel buffer**
          - **TDC unit**

- **Trigger module**
  - **L2 data**
  - **L2 data**

- **Data transmit**

if L2 was received.
Performance evaluation
Timing resolution

Timing distribution
between ch1 and common stop

Timing resolution
between each channel and common stop

Timing resolution better than 30 ps (σ) achieved for all the channel!
Double hit resolution

Double pulse could be measured with 100% efficiency.

In principle, double pulses with quite short interval can be measured.

Input pulse

Measured timing distribution

Leading edge timing [ns]
Double hit resolution

In principle, double pulses with quite short interval can be measured.

High-resolution multi-hit TDC was successfully developed.

We overcame HR-TDC problem in our field!
ToDo

Implement both leading and trailing edges measurement.
• At present, 8ch leading/trailing measurement was achieved.

Implement HR-TDC to FPGA on mezzanine card.
• Separate HR-TDC part from the DAQ functions.
• Customization of DAQ functions can be easy.

Future possibility
• Synchronization with master clock
• Implement as free-run type TDC

New mezzanine card for HR-TDC
(Same FPGA is mounted)
Summary

• Develop the 2nd level trigger system using FPGA based HR-TDC for the $K^+$ selection in J-PARC experiments.
• Furthermore, FPGA based HR-TDC solve the problem that no good HR-TDC exists in our research field.

• Tapped delay line HR-TDC, which realized by carry line, was implemented into Xilinx Kintex7 160T.
• 32ch HR-TDC unit and DAQ functions were fully implemented.

• The timing resolution better than 30 ps ($\sigma$) was achieved for all the channel.
• The double-hit resolution was at least 8 ns.

• We overcame the HR-TDC problem by this development.
Backup
Principle of calibration using clock.

clip at every 1.92 ns

Projection to Y
LUT Entry dependence of timing resolution

Timing resolution of ch0-ch1 (NIM)

Timing resolution of ch2-ch3 (ECL)

At present, LUT table accumulate 0x7ffff events.
Bit length dependence of timing resolution

Timing resolution of ch0-ch1 (NIM)

Timing resolution of ch2-ch3 (ECL)

At present, lower 8 bits are discarded.