~~汎用のメモリーモジュール、~~
高速TDC, ADCモジュール と将来の展望

大阪大学 岸本研究室
本多 良太郎

- Self-Introduction
- Overview of DAQ system
- Developed electronics
  - DRS4QDC
  - Hadron Universal Logic module
    - Its application
- Summary

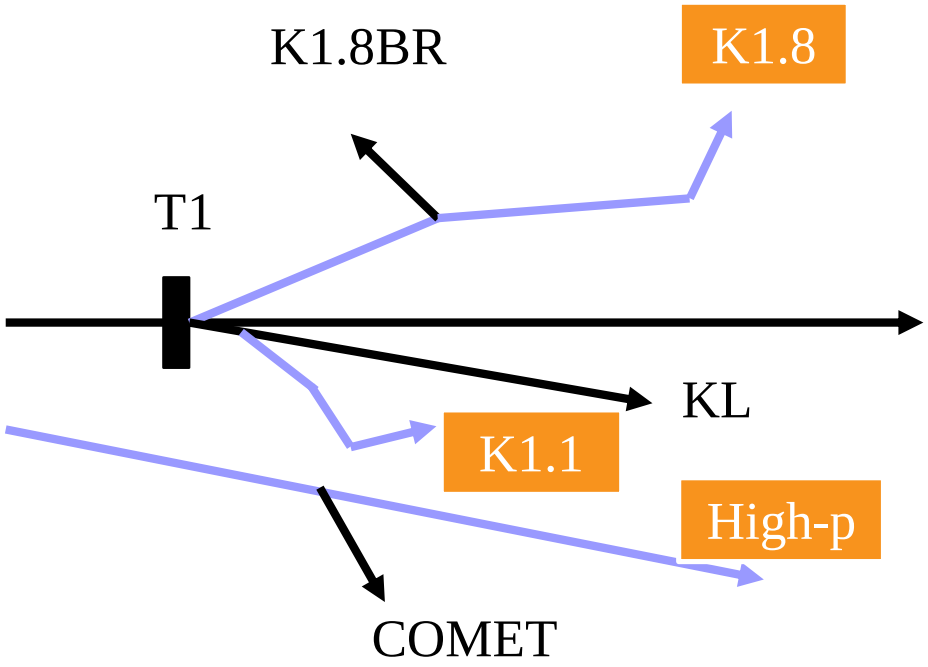
Self-Introduction

Ryotaro Honda （本多良太郎）
Strange nuclear physics, Hadron physics in J-PARC
Tohoku U. (Ph.D) → Osaka U. (PostDoc)

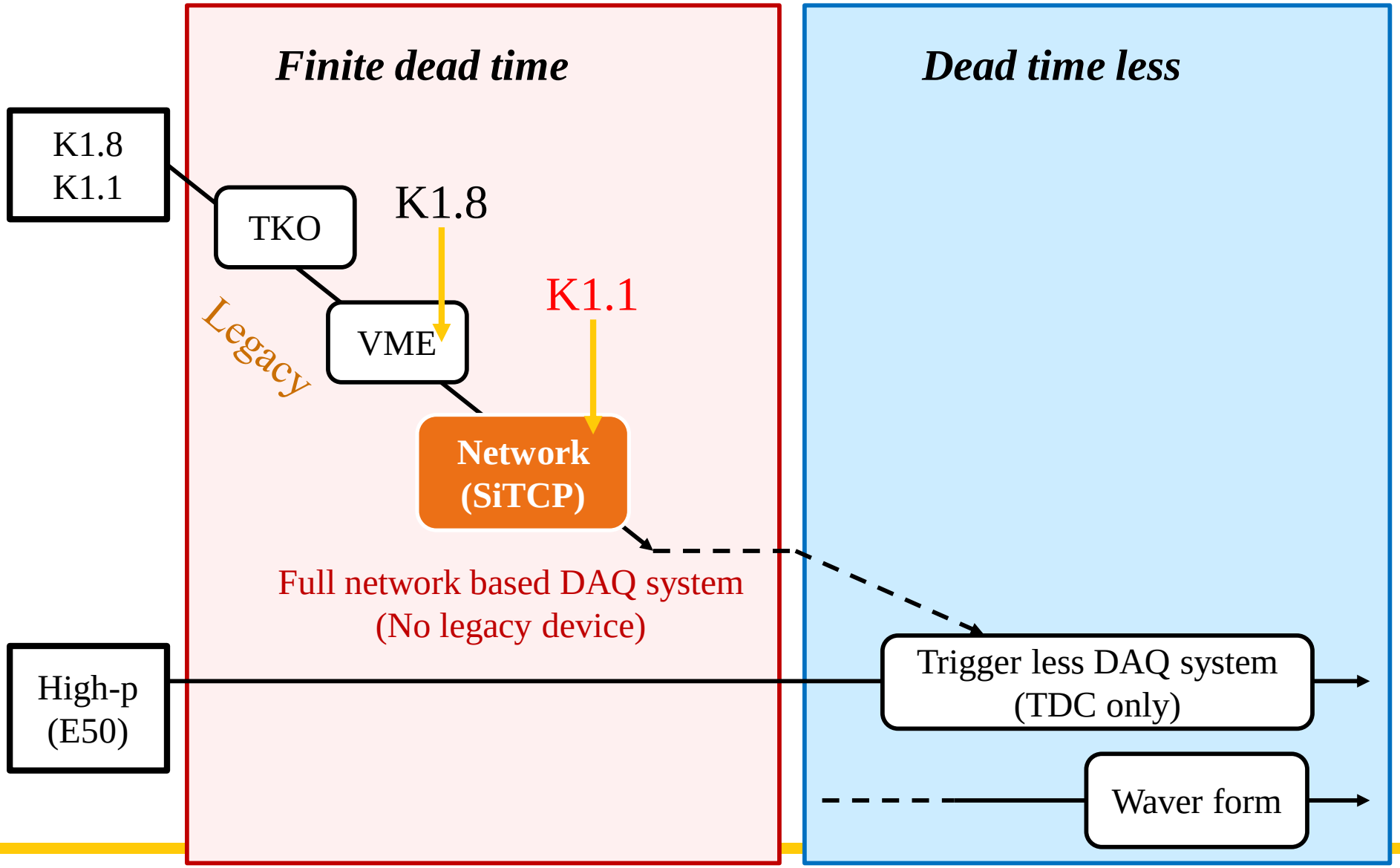
DAQ developer in K1.8/K1.1/ High-p beamline
Especially, for the hardware development.

- Circuit schema
- PCB design
- FPGA firmware
- (Software)

J-PARC Hadron facility



Dead time and generation of DAQ system



Detector setup in K1.1 (E63)

Timing (trigger) counters
- BH1
- BH2
- TOF wall
- SFV

Plastic scintillator

PID counters
- BAC1,2
- SAC1,3
- SP0
- SMF (LC)

Aerogel Cherenkov

Plastic scintillator

Lucite Cherenkov

Tracking detector
- BFT
- BC1,2
- SDC1,2,3,4

Scintillation fiber tracker

MWPC

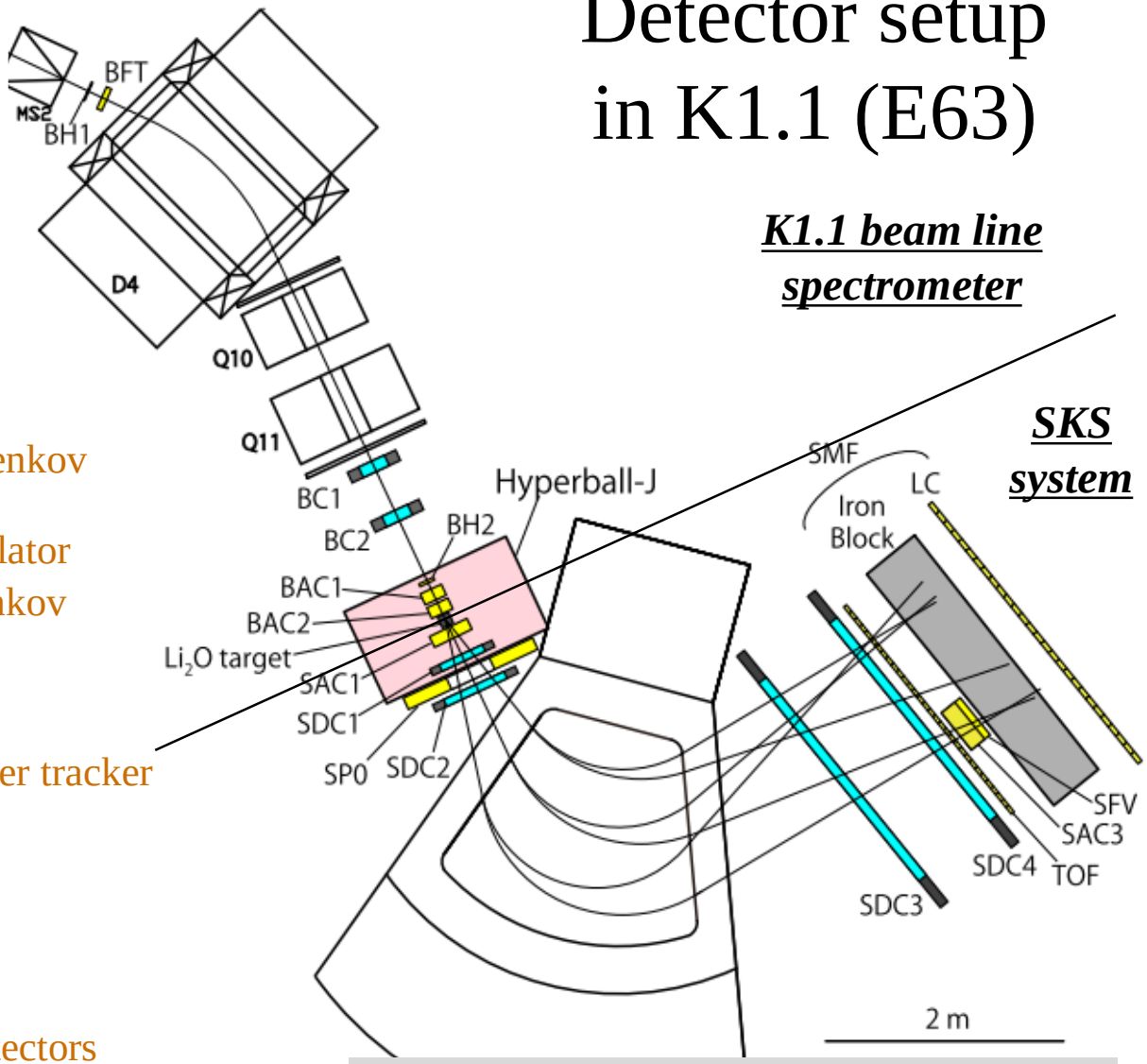
MWDC

γ-ray detectors
- Hyperball-J

Germanium detectors + PWO crystals

K1.1 beam line spectrometer

SKS system



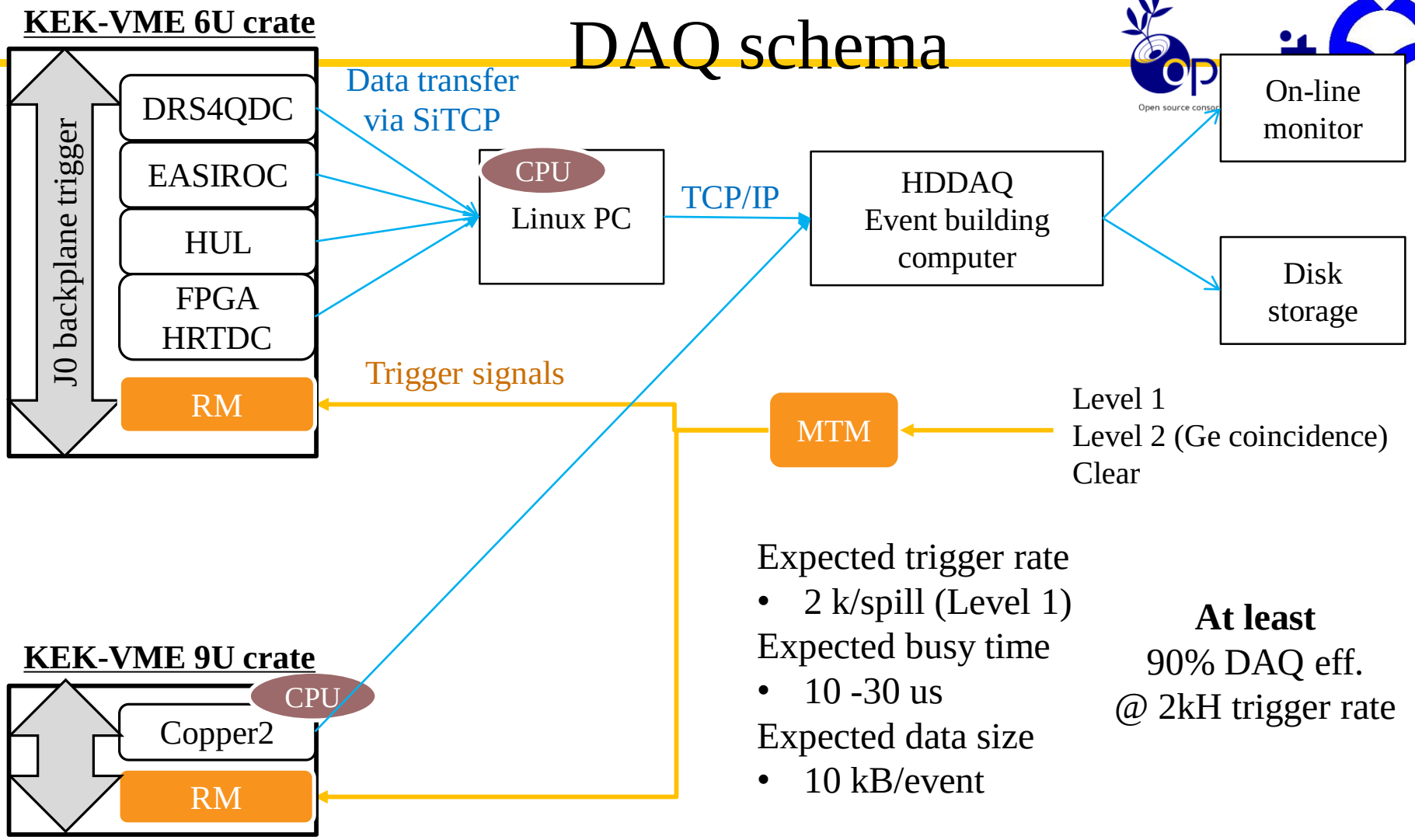
2.5 T (400A) for 1.1 GeV/c beam

List of detector specification and requirements

Detector	Device	# of ch	TDC	ADC	Electronics
Spectrometer systems					
BH1, 2, TOF	PMT	11+5+64	**High Reso.**	**YES**	**DRS4QDC** **FPGA-HRTDC**
ACs	PMT	27	Low Reso.	**YES**	**DRS4QDC**
SP0, SMF, SFV	PMT	80+56+6	Low Reso.	**YES**	**DRS4QDC**
BFT	MPPC	512	Low Reso.	No	**VME-EASIROC**
BC1,2	Wire chamber	3072	Low Reso.	No	Copper2
SDC1, 2	Wire chamber	576+448	Low Reso.	No	**HUL**
SDC3, 4	Wire chamber	1392	Low Reso.	No	**HUL**
Hyperball-J					
Ge	Ge	32	Low Reso.	**YES**	AD413A **HUL**
PWO	PMT	238	Low Reso.	(NO)	**HUL**

Only 80 ch need high-resolution TDC while a lot of low-resolution TDC are necessary.
Cost per channel in LR-TDC is a matter of concern.

DAQ schema



Expected trigger rate
- 2 k/spill (Level 1)

Expected busy time
- 10 -30 us

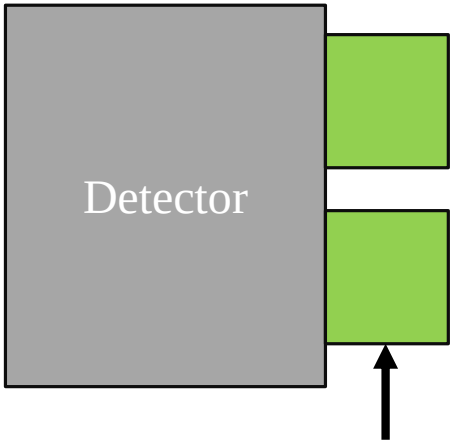
Expected data size
- 10 kB/event

At least
90% DAQ eff.
@ 2kH trigger rate

Front-end process of HDDAQ are running on the machine with CPU mark

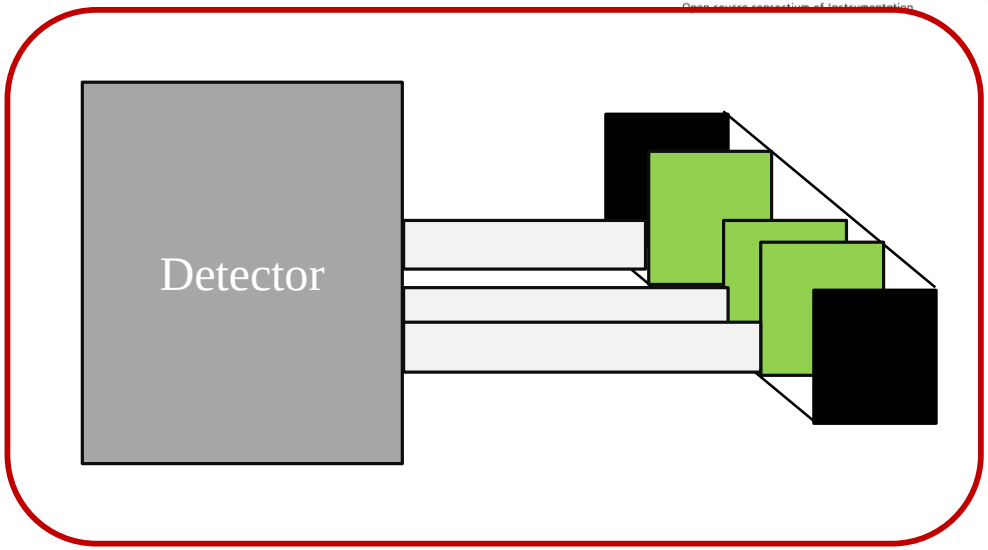
Almost the same as the K1.8 system, but all the electronics must be developed except for copper2.

Direct connection OR housing



読み出し回路

専用ビームライン
常設検出器に有効



汎用ビームライン
様々な検出器を読む場合に有効

K1.8ビームラインの実験リスト
E19, E27, E10, E13, E05, E07,
E03, E40, E42, E45, E22

安く・シンプル・運用が楽
なモジュールを作らなくてはいけない

ADC

DRS4QDC

Analog

- Number of channel 16
- Input range 2 Vp-p
- Common mode input range ±1 V
- Absolute input range ±2.8 V
- Buffer range 2 μs @ 1 GSPS

Digital I/O

- Discriminator outputs (LVDS), 16 ch parallel
- NIM level I/O (4 inputs, 2 outputs)
- Receive triggers from the KEK-VME J0 bus

Data transfer & control

- TCP & UDP realized by SiTCP (100 Mbps)

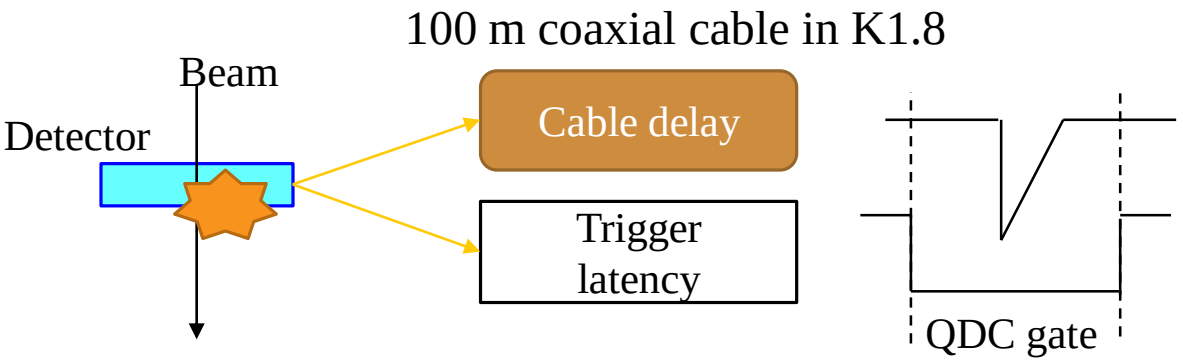
PCB standard

VME 6U KEK VME
Only J0 is mounted

- ±3.3 V from J0
  - +3.3 V ~ 4.2 A
  - -3.3 V ~1.8 A

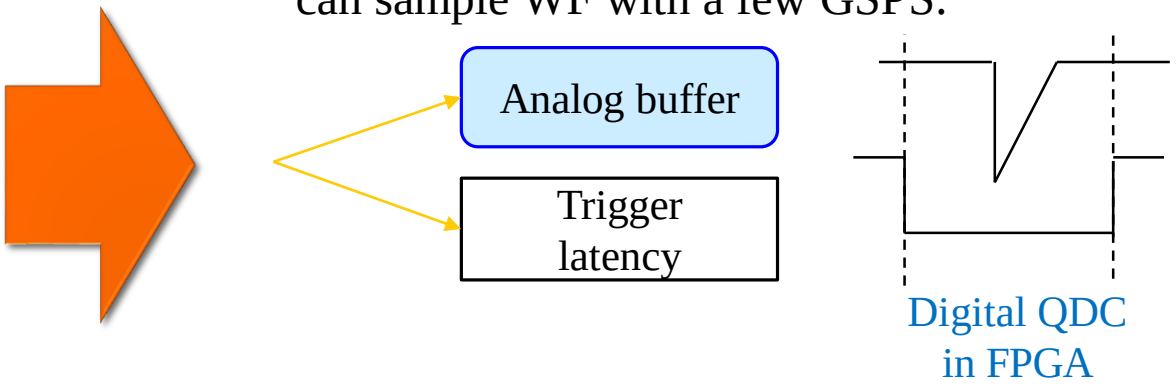
Open source consortium of Instrumentation

Motivation of DRS4QDC



Cable delay is unrealistic in future experiment.

- Expensive.
- Trigger latency is strongly limited.
- Not suitable for multi-channel.

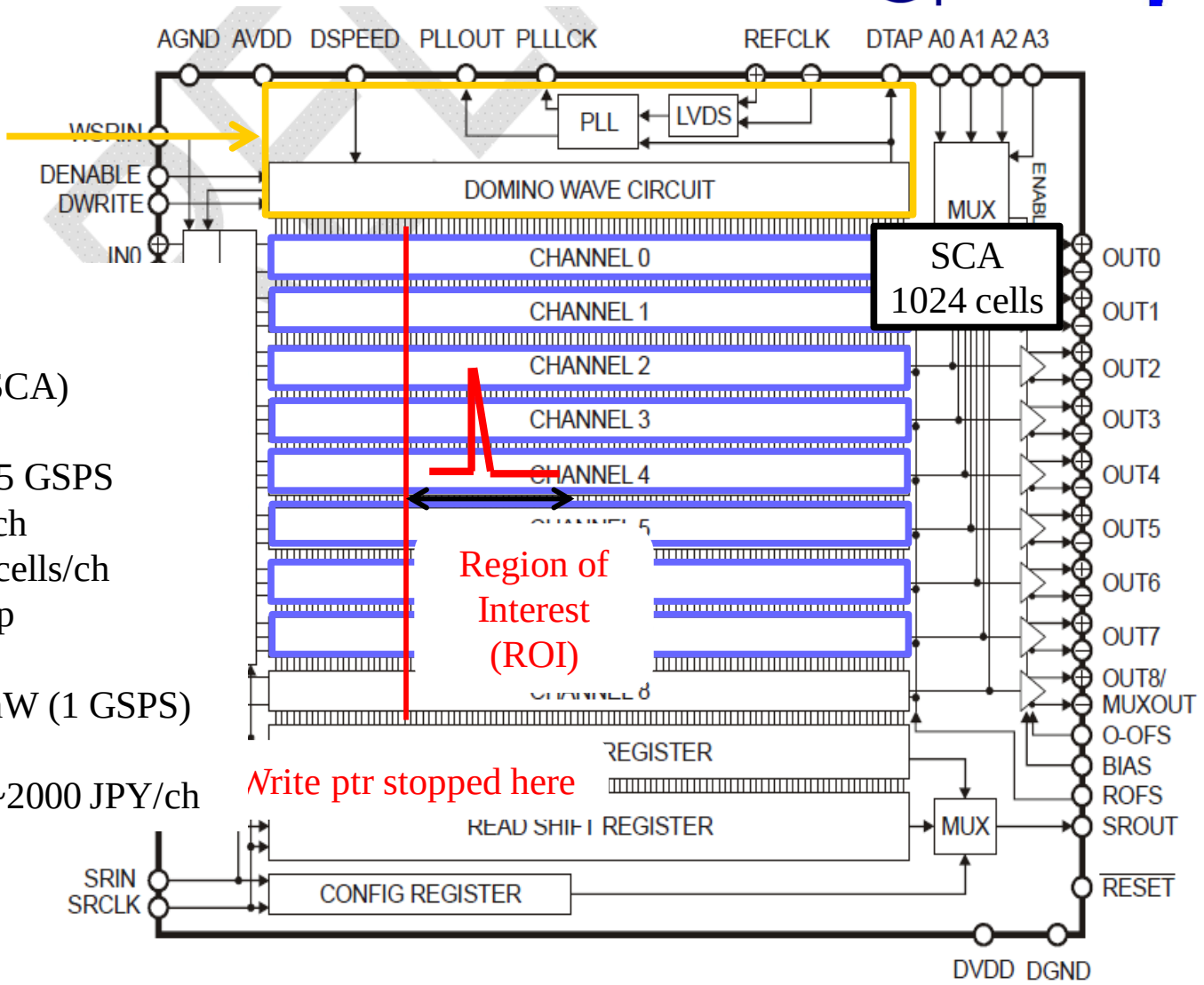


DRS4 – Method of sampling

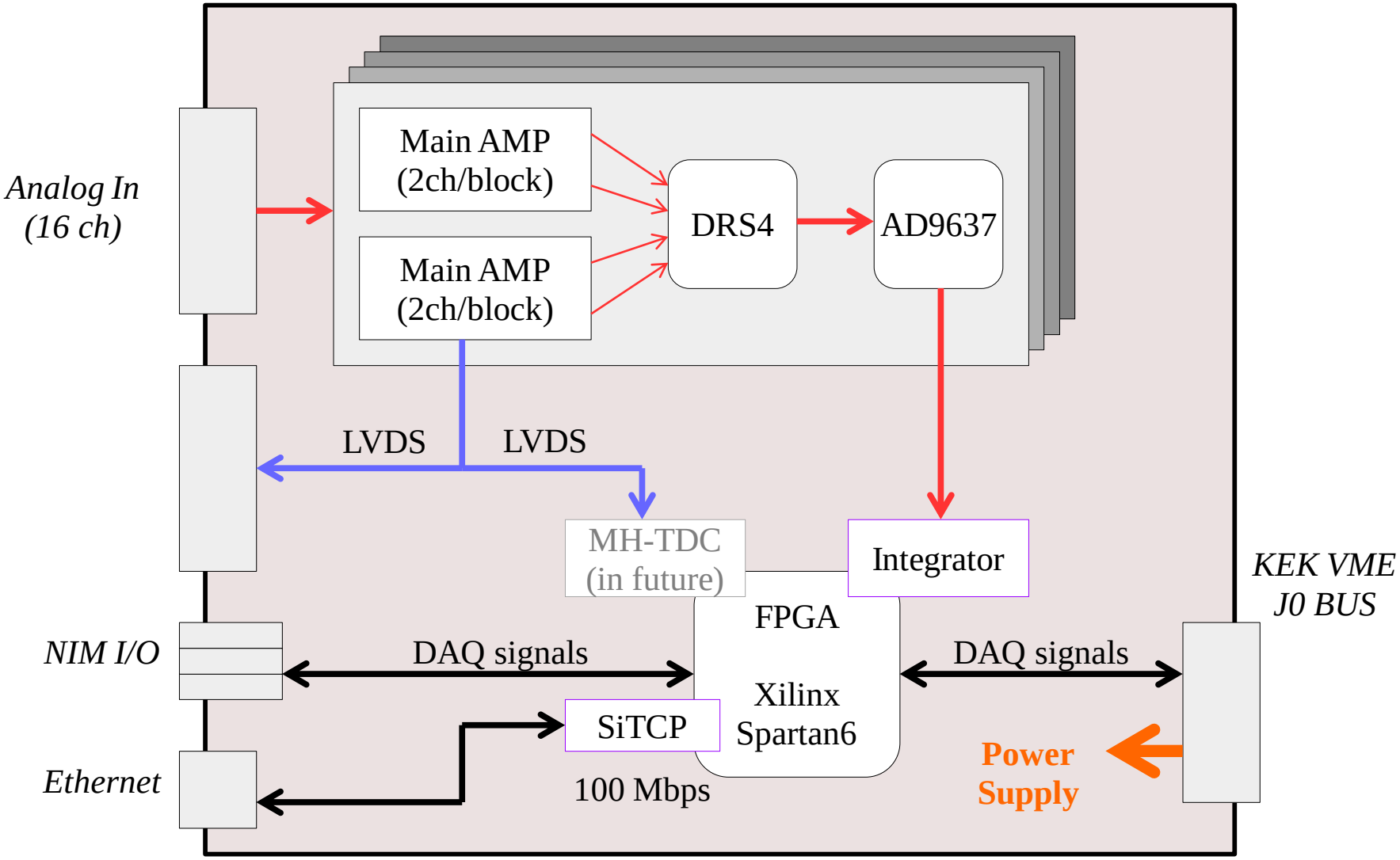
Domino wave
0.7 ~ 5 GSPS

Analog buffer
DRS4 (Developed by PSI)
Switched Capacitor Array (SCA)

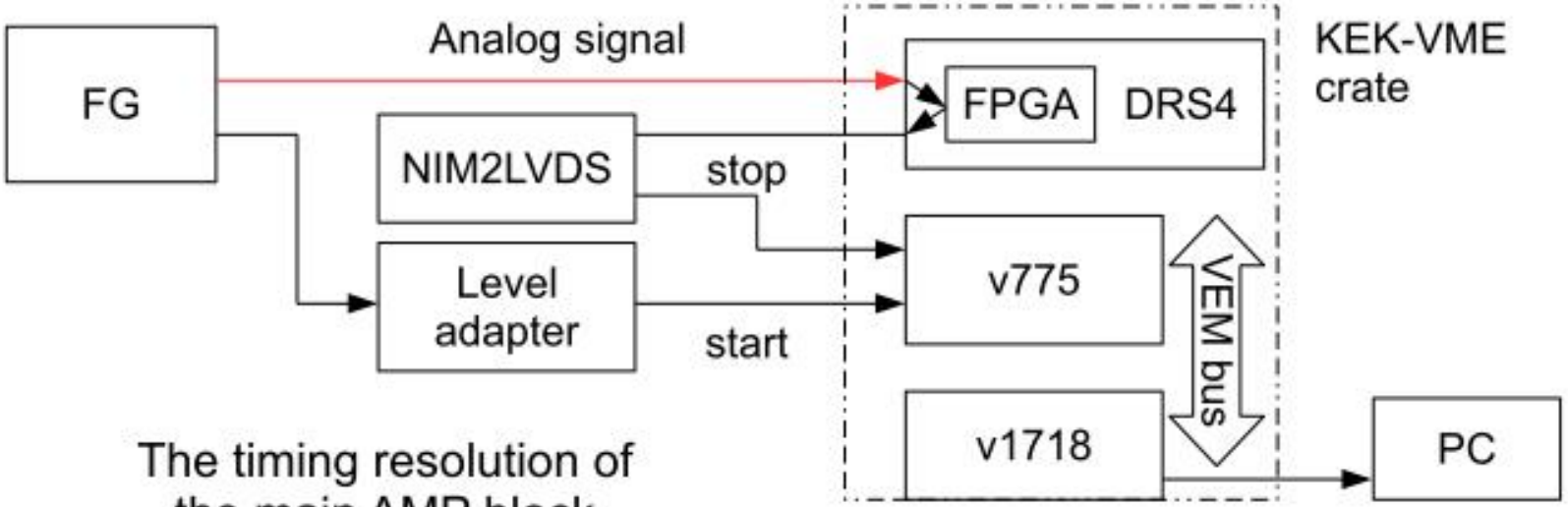
Sampling rate	0.7 ~ 5 GSPS
Input ch	8 (9) ch
Number of cells	1024 cells/ch
Input range	1 Vp-p
Power consumption	110 mW (1 GSPS)
Cost	1000~2000 JPY/ch



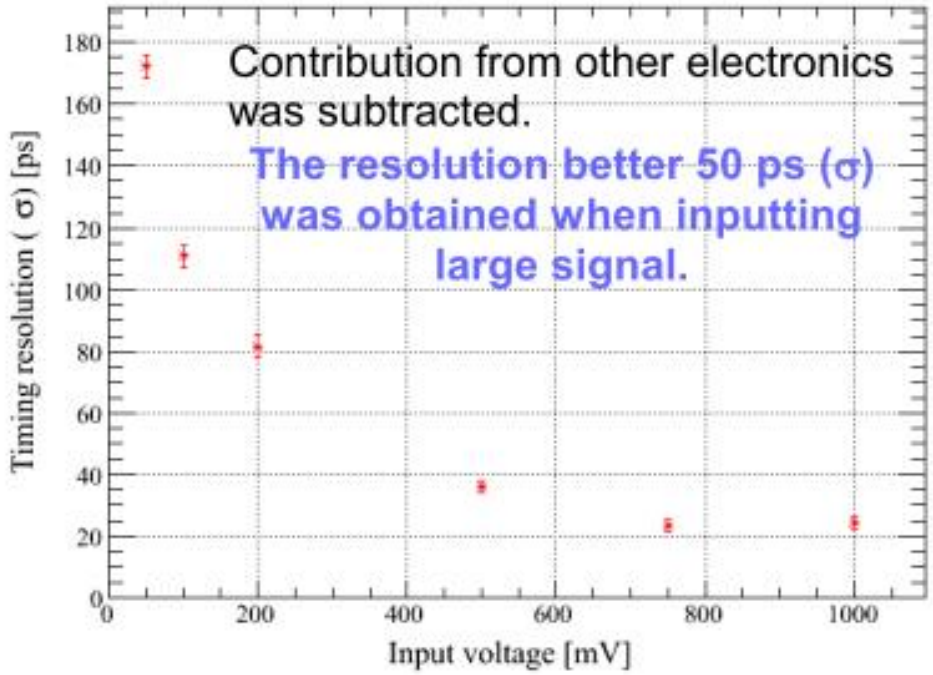
DRS4QDC block diagram



Performance evaluation
– Timing resolution of Main AMP block



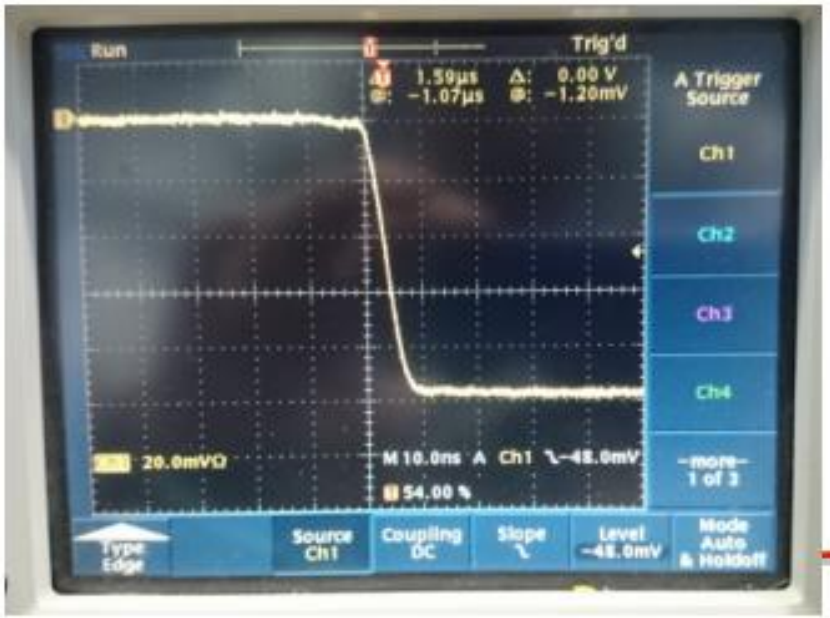
The timing resolution of the main AMP block



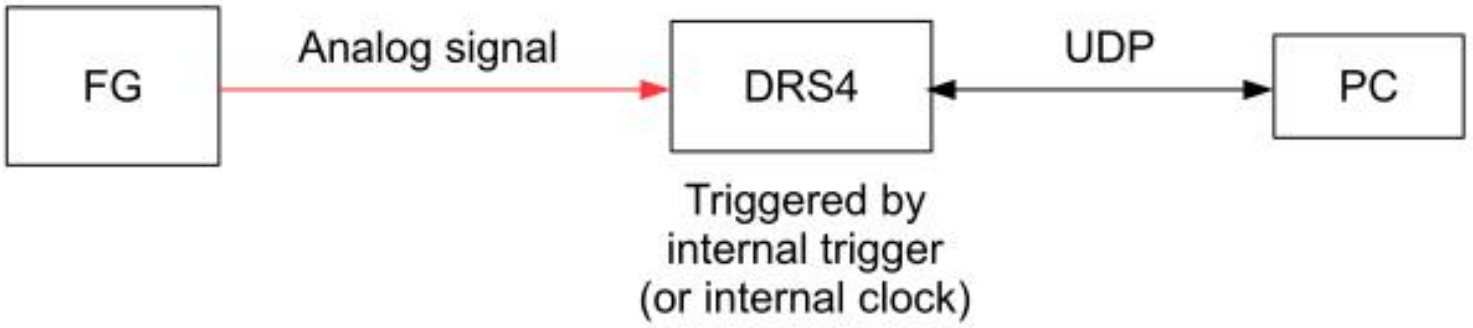
Contribution from other electronics was subtracted.

The resolution better 50 ps (σ) was obtained when inputting large signal.

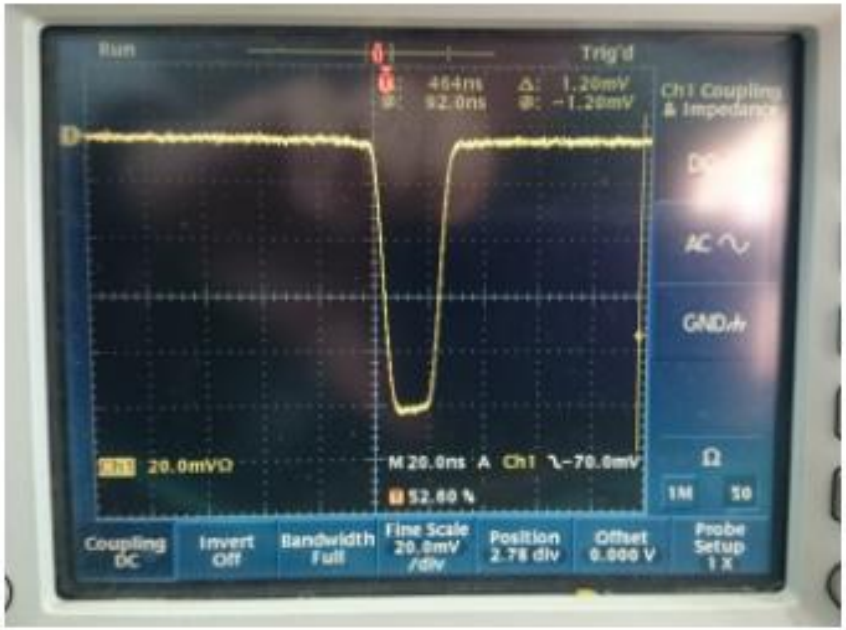
Input signal



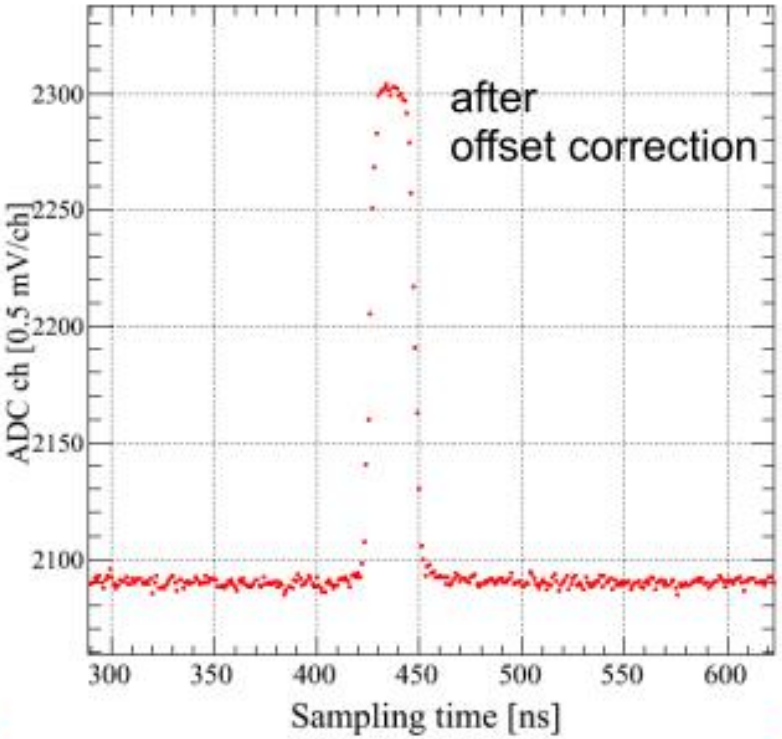
Performance evaluation – Waveform



The input signal
(100 mV & 20 ns width)



Readout result



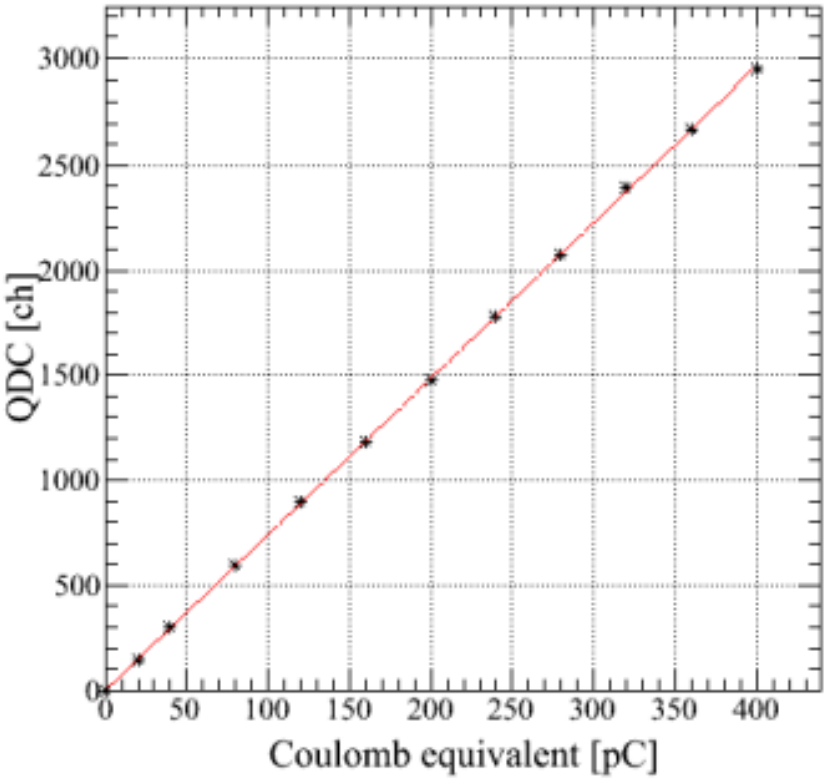
Performance evaluation – QDC

The measurement of the linearity of this system by changing the signal height.

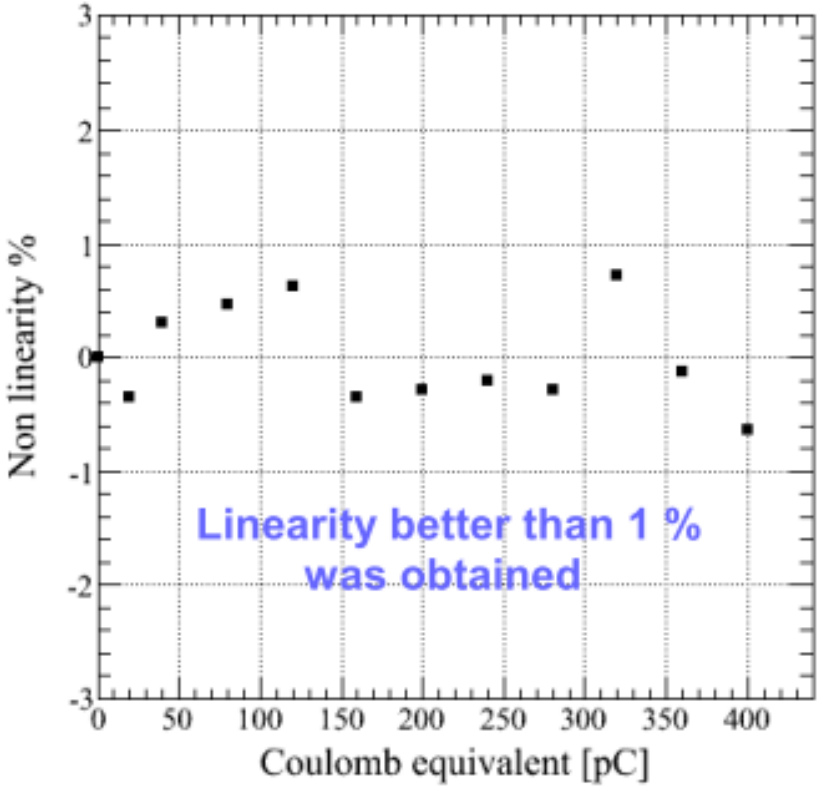
Definition of non linearity

Non linearity = (QDC mean – f(x))/(QDC mean) x 100

Mean position vs input charge



The distribution of non linearity



Specification

Analog

Number of channel	16
Input range	2 Vp-p
Common mode input range	±1 V
Absolute input range	±2.5 V
Buffer range	2 μs @ 1 GSPS
QDC LSB	**0.135 pC/ch**
QDC Linearity	**< 1 %**
QDC noise level	**2.7 ch (σ) for pedestal**
QDC resolution	**~ 0.9 %**

Digital I/O

Discriminator outputs (LVDS), 16 ch parallel

Timing resolution	**< 50 ps (s)**

NIM level I/O (4 inputs, 2 outputs)

Data transfer & control

TCP & UDP realized by SiTCP (100 Mbps)

PCB standard

VME 6U KEK VME

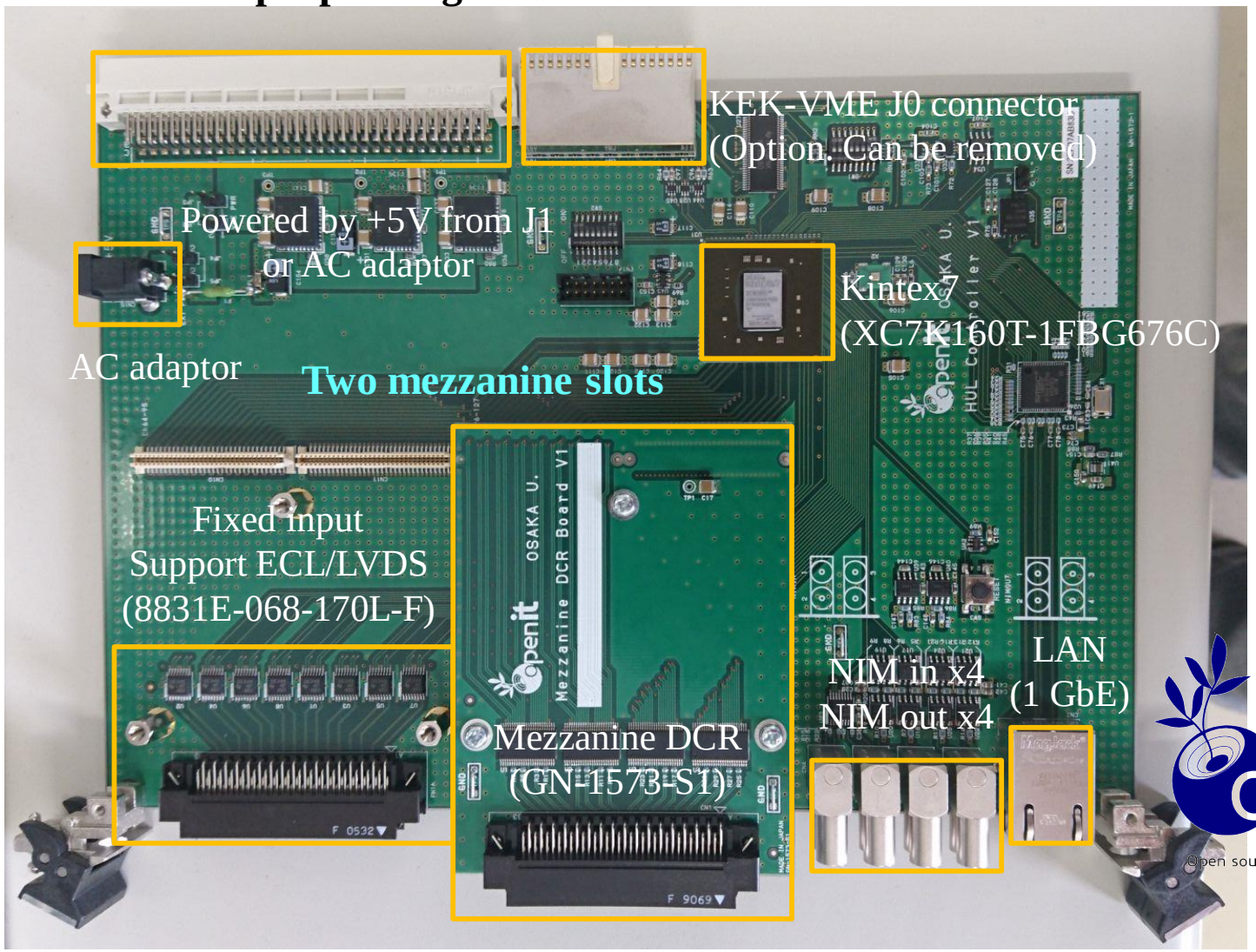
Only J0 is mounted

If you have an interest, please contact us!

TDC

Hadron Universal Logic (HUL) module specification

General purpose logic board with Kintex7 and SiTCP



Fixed input (64ch) + Mezzanine (64ch in max.)

= 128ch direct connection to FPGA

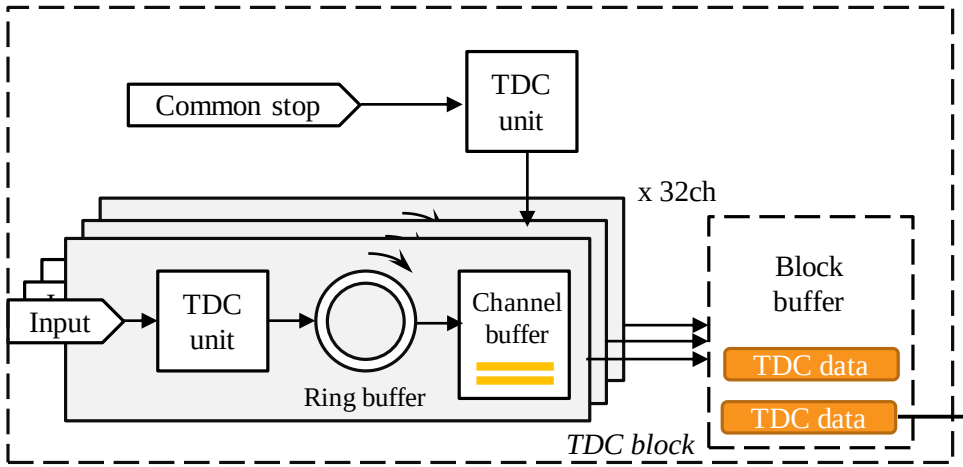
Requirements to new module

As cheep as possible
- Requirement : 1500 JPY/ch

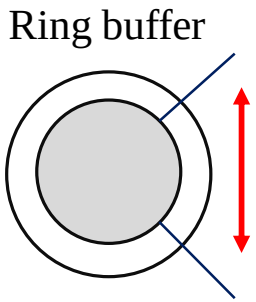
Data communication via TCP/IP
- Register setting
- Usage as DAQ module
- Downloading MCS file via network

Mount the mezzanine card slots
- Capability for various types of the signal standard
- Increase the maximum input channels up to 128 ch
- Extension to various kinds of applications

Example of application (Multi-Hit TDC)

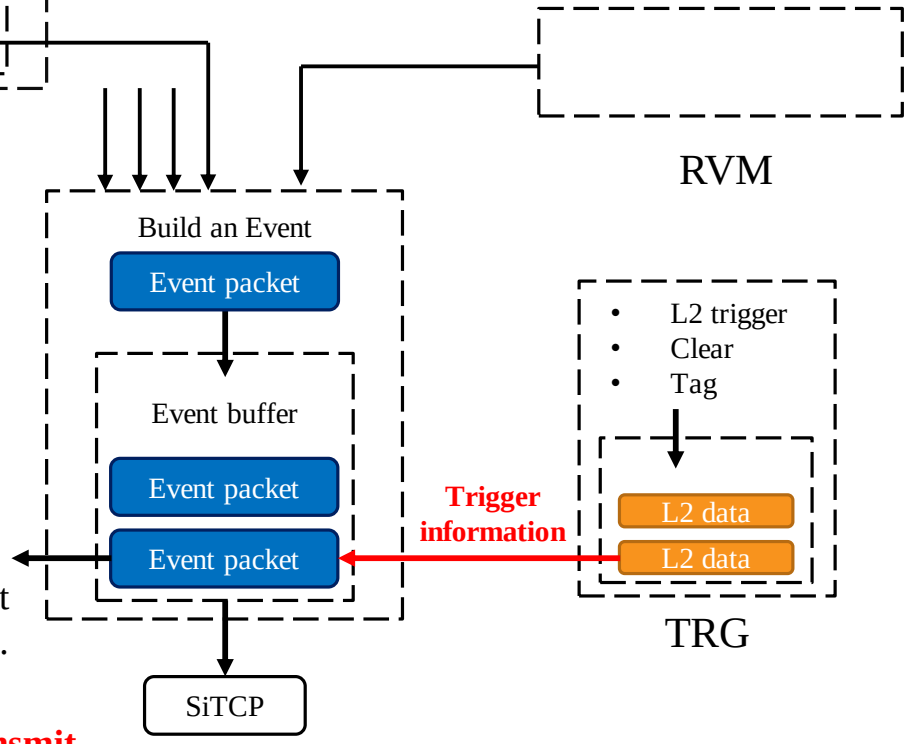


Multi-Hit TDC



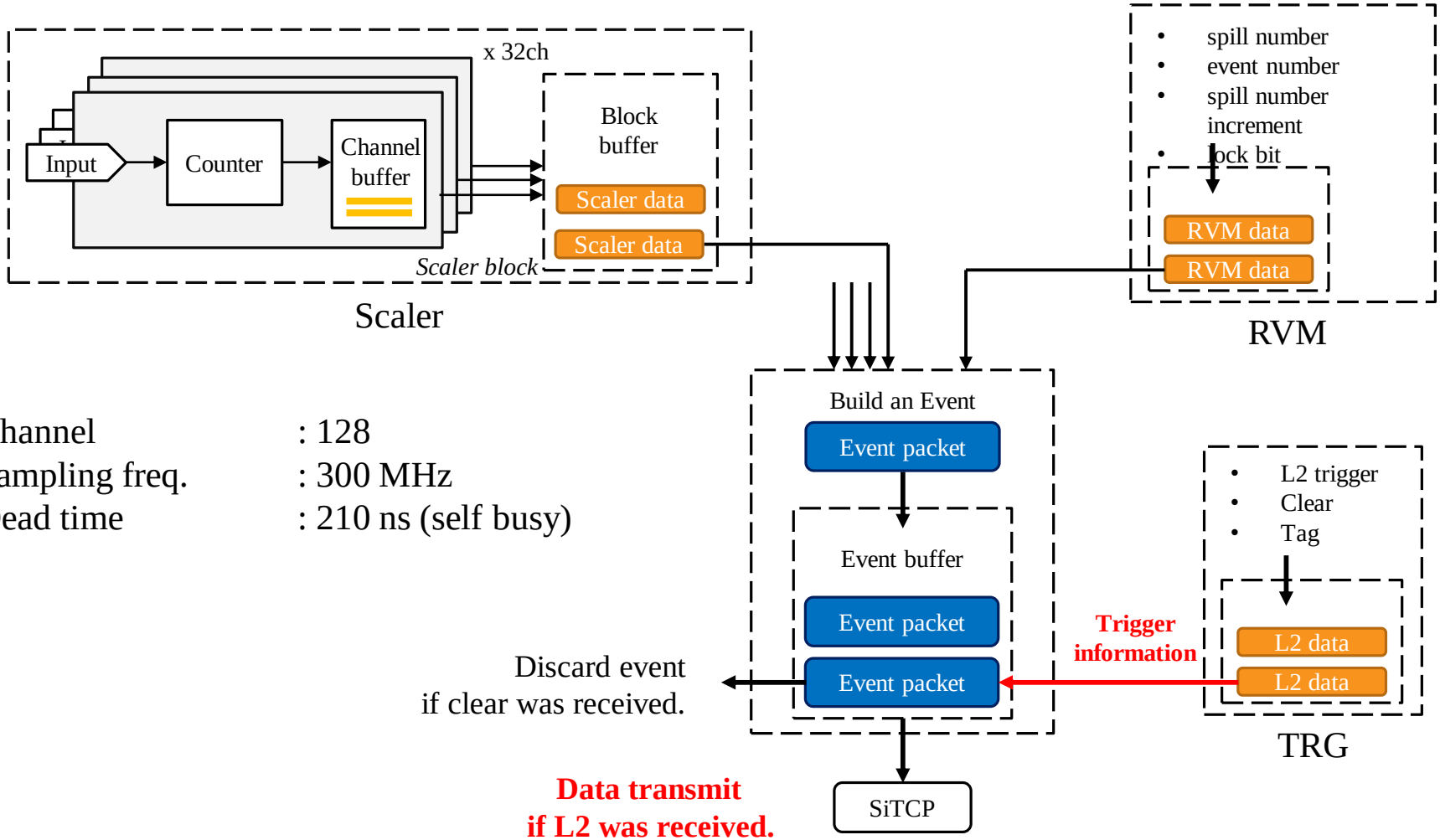
Hits inside the search window are stored in channel buffer, when trigger is received.

Channel	: 128
Trigger type	: Common stop
Ring buffer length	: 13.7 us
MaxHit/ch/event	: 16
Precision	: 0.83 ns
Resolution	: 300 ps (r.m.s)
Dead time	: Equal to search window



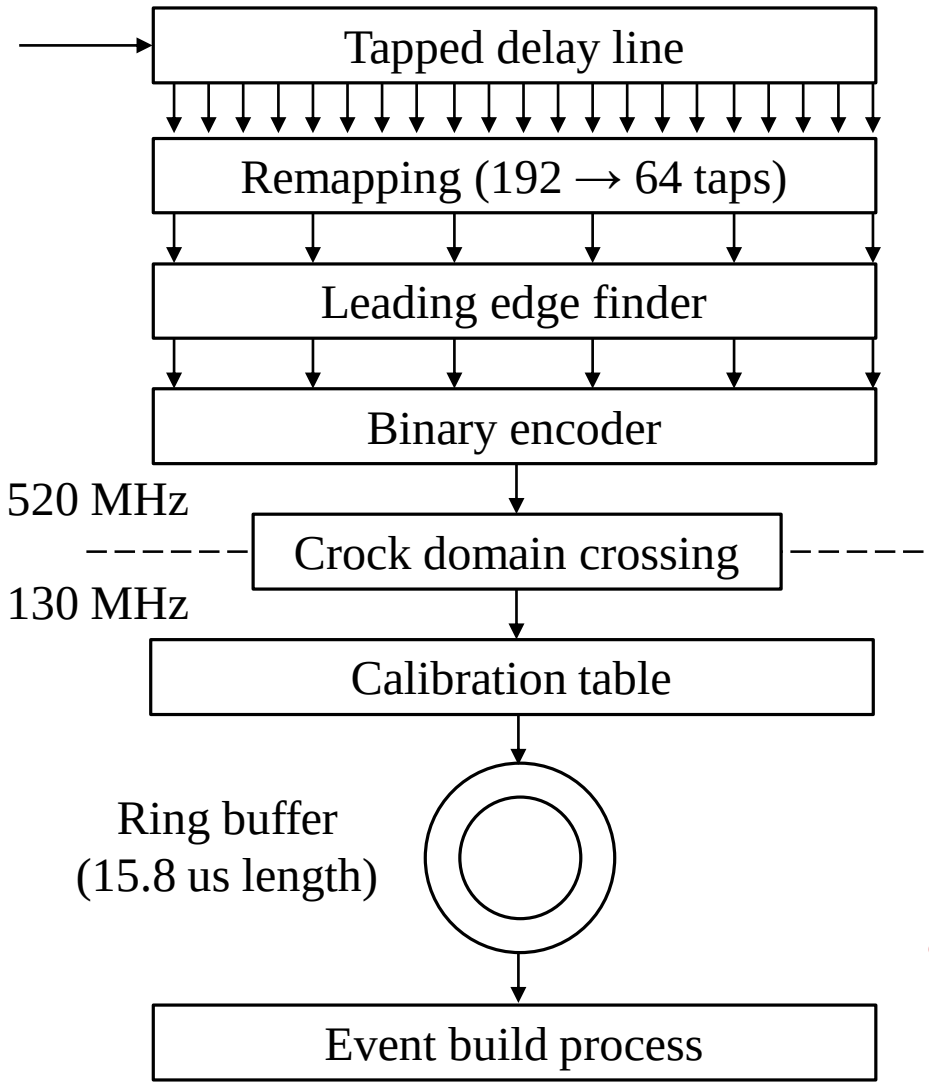
Data transmit if L2 was received.

Example of application (Scaler)



Channel : 128
Sampling freq. : 300 MHz
Dead time : 210 ns (self busy)

Implemented logic



Pulse run →

1111111111111000000000000000

1111100000

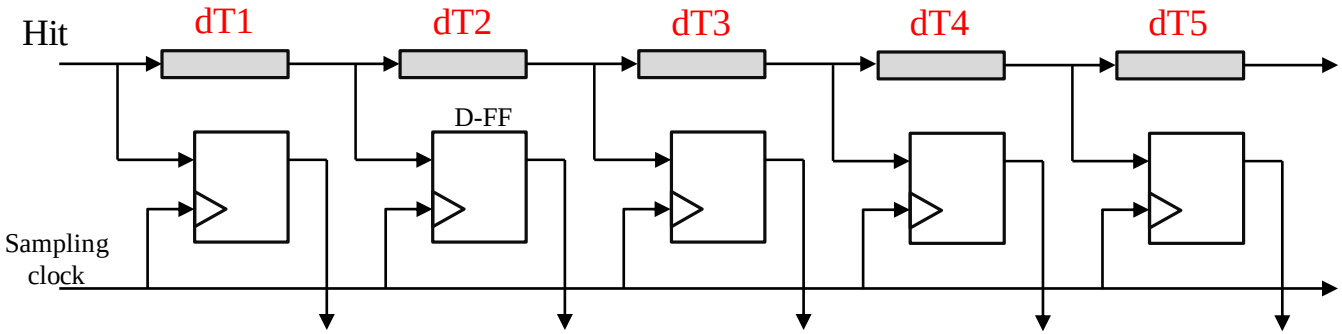
0000100000

5 : Fine count
+
Semi coarse count (2bit)
+
Coarse count (11bit)

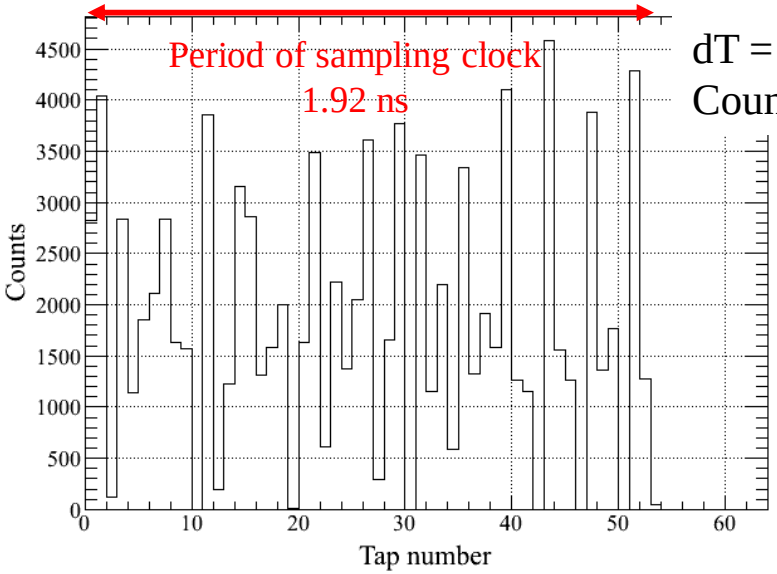
32ch leading HR-timing units
(or 16ch leading/trailing HR-timing units)
and DAQ functions were fully implemented into Kintex7 160T.

Distribution of delay time

Delay time (dT) is not constant.

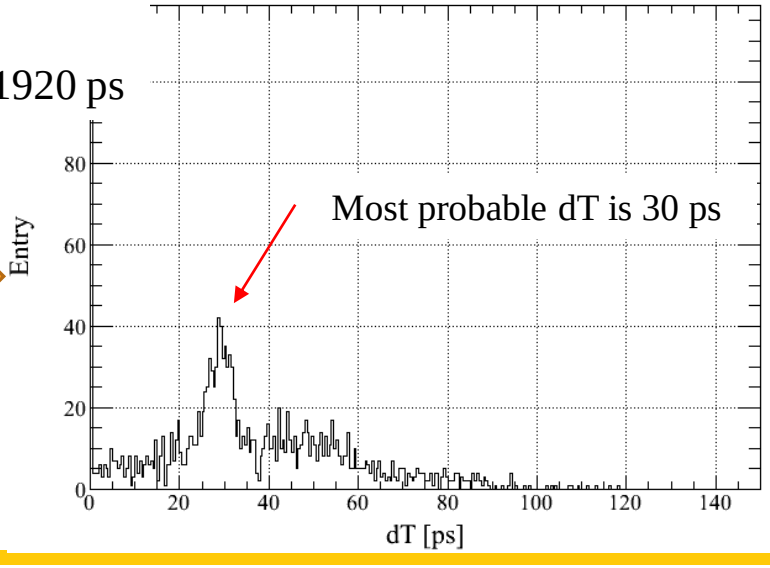


Tap number histogram

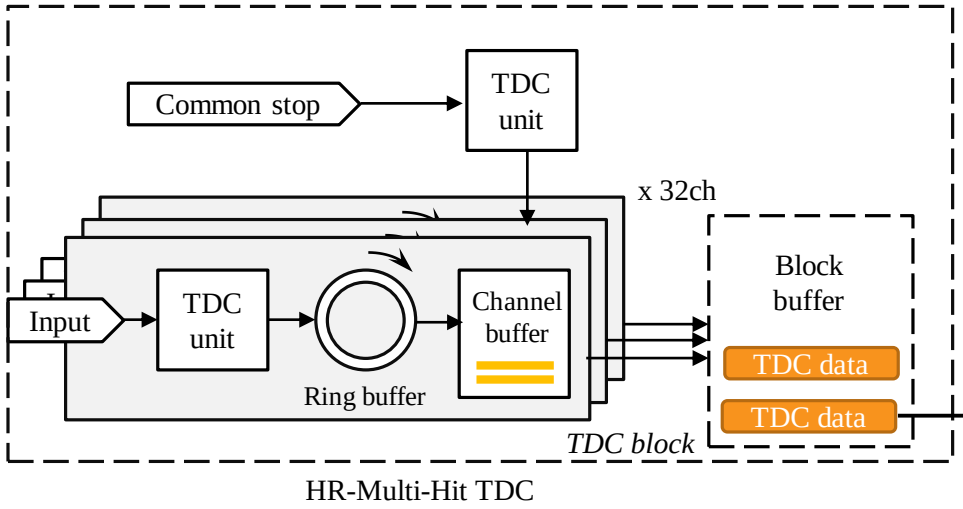


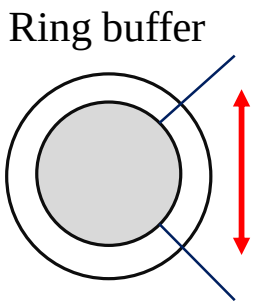
dT = Count/TotalEntry*1920 ps

dT distribution for all the channels



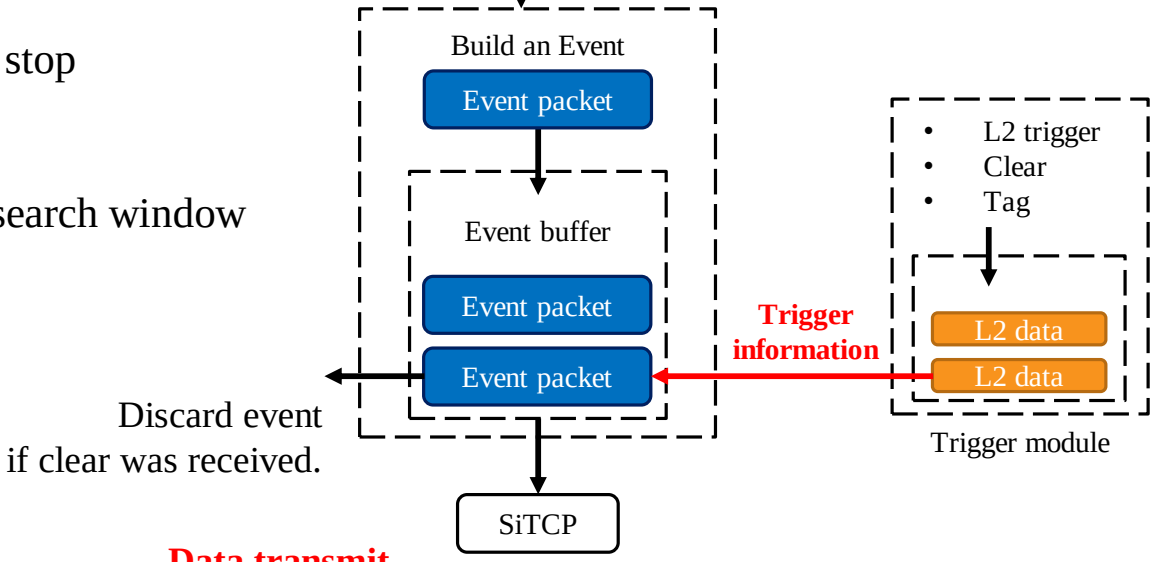
DAQ functions





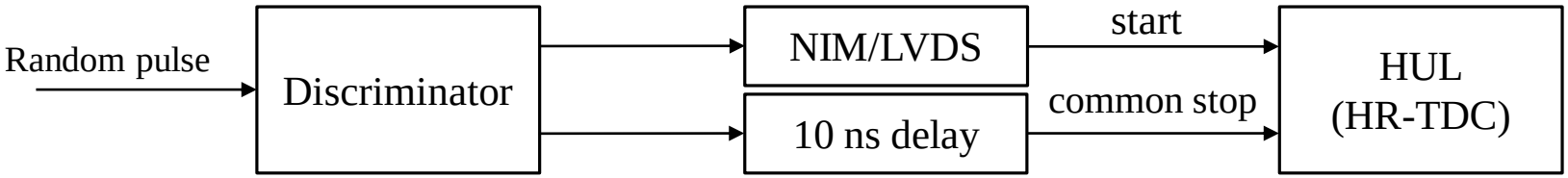
Hits inside the search window are stored in channel buffer, when trigger is received.

Channel : 32
Trigger type : Common stop
Ring buffer length : 15.8 us
MaxHit/ch/event : 16
Dead time : Equal to search window

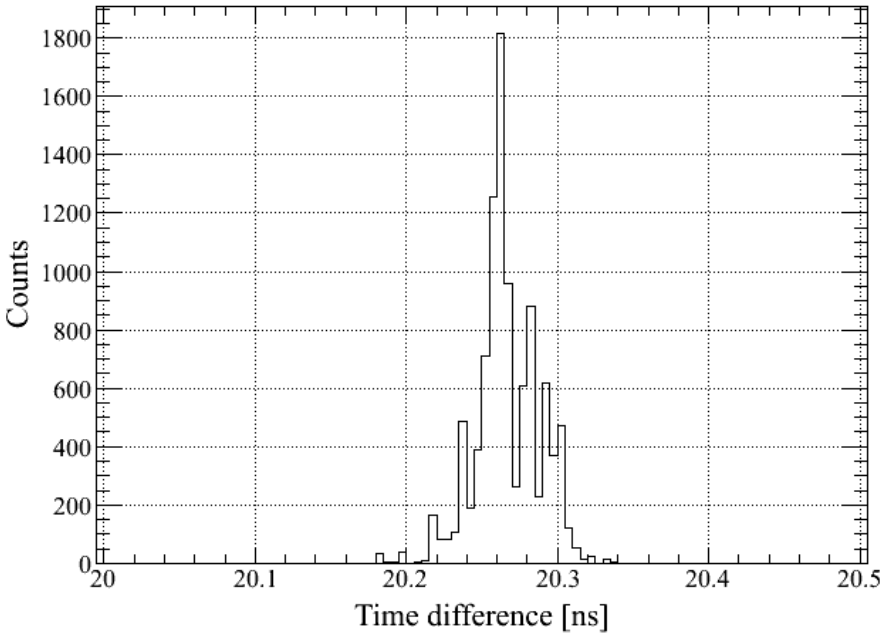


Data transmit if L2 was received.

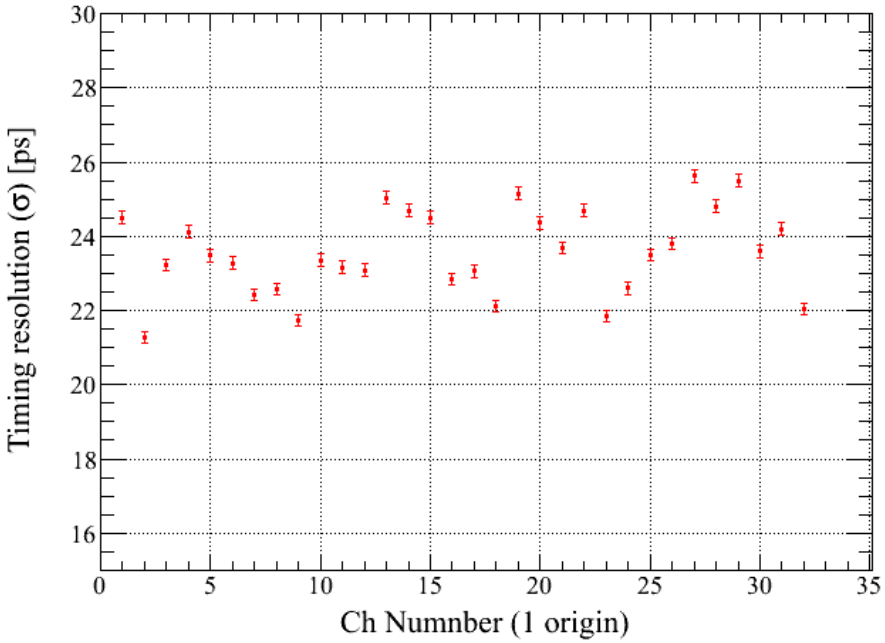
Timing resolution



Timing distribution
between ch1 and common stop



Timing resolution
between each channel and common stop



Timing resolution better than 30 ps (σ) achieved for all the channel !

ToDo

Implement HR-TDC to FPGA on mezzanine card.

- Separate HR-TDC part from the DAQ functions.
- Customization of DAQ functions can be easy.

Future possibility

- Synchronization with master clock
- Implement as free-run type TDC

New mezzanine card for HR-TDC
(Same FPGA is mounted)

将来の展望

常設検出器(TOFやWire chamber等必ず必要な検出器)

ADC (QDC)用の技術

- DRS4-QDC → コスト・運用に難あり
  - 1-3 MHz/chに対応可能なPMT用の電荷読み出し技術を考えれないか？
  - 単純なQDCではパイルアップするため非現実的。

TDC技術

- FPGA low-resolution TDC
- FPGA high-resolution TDC
  - 50ps (σ)程度までの検出器であれば開発した技術で十分か？
  - 実装方法の改善で分解能15 ps (σ)程度まではいけるかも。

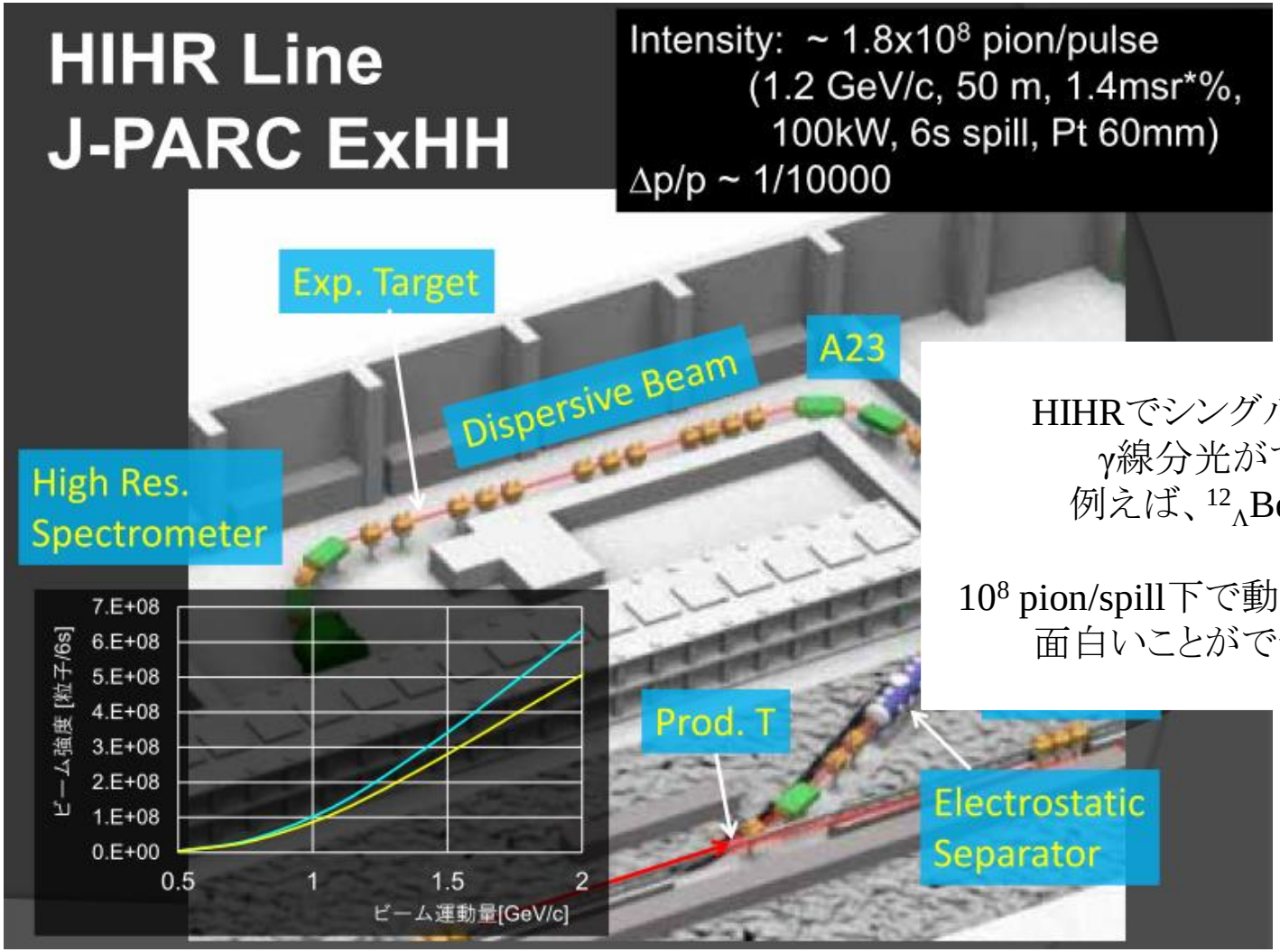
多チャンネルMPPC読み出し

- VME-EASIROC → 電荷読み出しに難あり
- **TOTによる電荷測定**ができたら将来Cylindrical Scintillation Fiber Tracker（E40）のアップグレードに利用可能。（午前中の質問に対応：1-10 pCで100 kHz）

崩壊事象検出器(γ線検出器など)

- 未着手
  - **高BG下で動くγ線検出器を実現できないか？**

HIHR（ハドロンホール拡張後）におけるγ線検出



HIHRでシングルΛハイパー核の
γ線分光ができないか？
例えば、$^{12}_{\Lambda}$Be (1 MeV以下)

10^8 pion/spill下で動くγ線検出器があれば
面白いことができないだろうか？

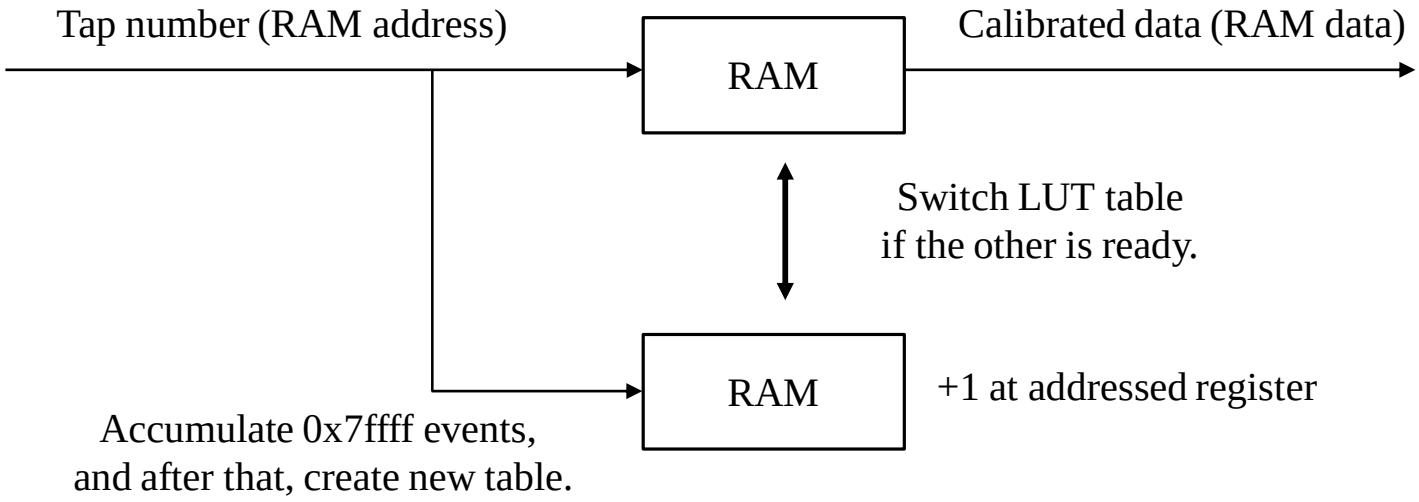
Summary

Construct the full network based DAQ system for the existing and future beam line.

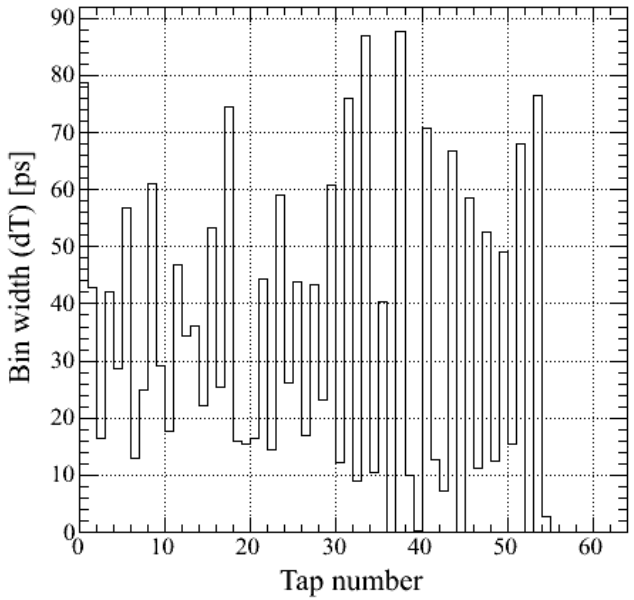
Developed items

- DRS4-QDC
  - 16ch input
  - 1 GSPS : 2 us buffer
  - 50 ps (s) timing resolution of main AMP.
  - QDC precision 0.135 pC/ch
  - QDC linearity < 1%
- Hadron Universal Logic module
  - Multi-Hit TDC (0.83 ns precision)
  - 300 MHz scaler
  - FPGA based HR-TDC (30 ps precision)

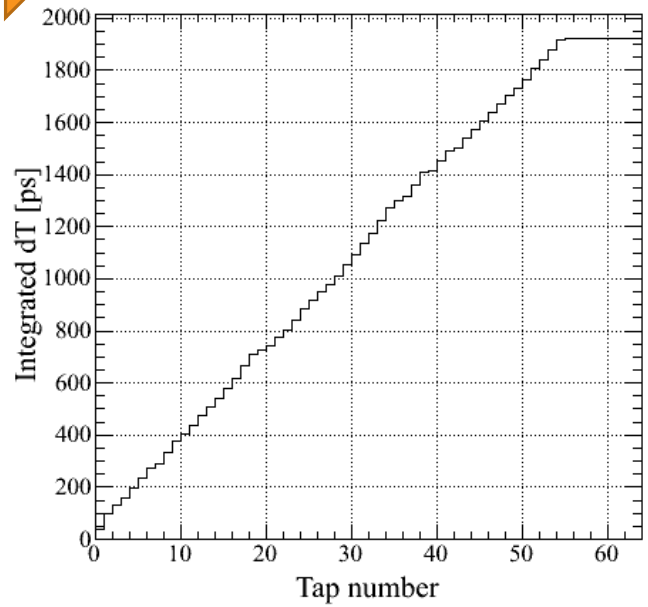
Calibration of TDL



Tap number histogram



Calibrated look up table



Nth Val =
$w_n/2 + \Sigma^{n-1}_0 (w_i)$

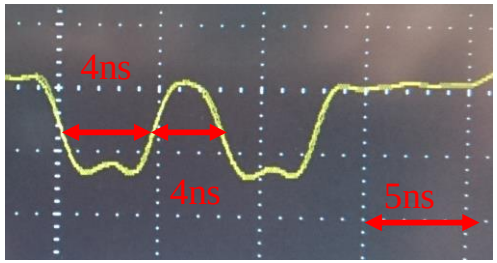
Calibration of method

- Use detector signal.
  - Corresponding to that the clock sampling of the detector signal. The detector signal must be random.

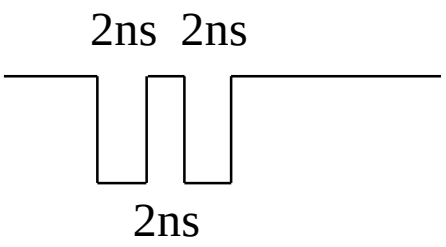
- Use clock.
  - The TDC clock is 520 MHz (f_{sample}) and calibration clock is 26.2144 (f_{calib})
  - $N*(f_{sample}/f_{calib}) = N*(2^{9}*5^{7}*13)/(2^{20}*5^{2}) = N*(5^{5}*13)/\mathbf{2^{11}}$
  - 2048 different clock phases appear

Double hit resolution

Input pulse



Double pulse could be measured with 100% efficiency.



In principle, double pulses with quite short interval can be measured .

Measured timing distribution